Ref.No. IGBT-01 (Rev.2)

IGBT MODULE

Application Manual

Hitachi, Ltd. Power & Industrial Systems
Power Semiconductor Dept.
Power & Industrial Systems Div.

1 Introduction to Hitachi IGBT Modules

This application manual references specifications of the GS Series AW Version of Hitachi Insulated Gate Bipolar Transistor (IGBT) modules. For detailed information and specifications for the entire product line, refer to the **Hitachi IBGT Module Data Manual** or access the index of information at the Hitachi World Wide Web site *http://www.hitachi.co.jp/Div/ise/pdevice/index.htm*.

1.1 New Generation of High-Power IGBT Modules

IGBT applications are rapidly expanding. Since they make possible higher efficiency and quieter operation of equipment such as general-purpose inverters, uninterruptible power supplies, and welders, IGBTs are now used in many diverse application areas. Recent development of 3.3 kV high-voltage IGBT modules expands their scope of applicability to fields such as traction motor control. Building on this experience, Hitachi presents a new, expanded range of high-power IGBT modules suitable for a variety of applications.

1.2 Inherent Design Concepts

High performance and high reliability combined with the use of improved ultra-soft and fast-recovery diodes are the underlying reasons why Hitachi high-power IGBT modules offer reduced power losses and noise that results in higher operating efficiency.

1.3 Application Areas

Listed below are areas where Hitachi's IGBT modules are currently finding wide acceptance.

- AC Servo Drive Systems
- Air Conditioners
- Converters
- Electric Vehicles
- Elevators
- Inverters
- Medical Equipment
- Robots
- Traction Motor Control
- Uninterruptible Power Supplies
- Welders

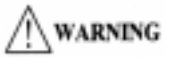
2 Precautions for Safe Use

Before attempting to apply any information contained within this Hitachi IGBT Modules Application Manual, please be certain to read the descriptions thoroughly regarding warning and caution symbols cited below.

In particular, always keep in mind the fact that failures may result if Hitachi IGBT modules are misapplied. So, if during such misuse an Hitachi IGBT module fails, it is possible that the IGBT module will emit smoke, cause a fire, or even burst.

2.1 Warning and Caution Symbols

The **EXCLAMATION** mark enclosed within a triangle indicates an item about which caution is required.



The **WARNING** mark indicates a potentially hazardous situation which, if not avoided, could result in death or serious injury.

The **CAUTION** mark indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury and/or damage to property.

CAUTION

(1) Regardless of changes in external conditions during use, "absolute maximum ratings" should never be exceeded when designing semiconductor-based electronic circuits. Furthermore, in pulsed-mode situations, "safe operating area (SOA)" precautions should always be observed.

(2) Hitachi IGBT modules may experience failures due to accidents or unexpected surge voltages. Accordingly, you should always adopt fail-safe design techniques, such as redundancy, to avoid extensive damage in the event of failure.

(3) For those cases where extremely high reliability is required (such as in applications involving nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment, and various kinds of safety equipment), extended safety measures should be taken to ensure maximum protection of personnel, environment, and the equipment and processes involved. This could include following user's fail-safe precautions, adoption of situation-specific safety arrangements, and consulting Hitachi America, Ltd.'s sales department staff.

2.2 Notices

1. This manual states what the application precautions are concerning IGBT modules.

2. This manual is subject to change without prior notice to accommodate technology changes which affect product characteristics.

3. In no event shall Hitachi be liable for any failure in an Hitachi IGBT module or any secondary damage resulting from use at a value exceeding the absolute maximum rating or that may result from an accident or any other cause based on the information in this applications manual. Hitachi assumes no responsibility for any intellectual property claims or any other issue that may result from applications information, products, or circuits described in this manual.

4. No license is granted by this manual under any patents or other rights of any third party or Hitachi America, Ltd.

5. This manual may not be reproduced or duplicated, in any form, in whole or in part, without the expressed written permission of Hitachi America, Ltd.

6. The products (technologies) described in this manual are not to be provided to any party whose purpose in their application will hinder maintenance of international peace and safety nor are they to be applied to that purpose by their direct purchasers or any third party. When exporting these products (technologies), all necessary procedures are to be taken in accordance with related laws and regulations.

7. In no event shall Hitachi be liable for any failure in a semiconductor device or any secondary damage resulting from use at a value exceeding the absolute maximum rating.

3 General Description of IGBT Modules

3.1 Part Numbering

Table 1 provides a specific example of the numbering system characteristics for Hitachi IGBT modules.

Table 1. Numbering System Characteristics

M	B	N	1200	GS	12	AW	Part Numbering Example
M							**Assembly IGBT module: (*IGBT modules* always an M)**
	B						**Classification of main component: (*IGBT modules* always a B)**
		N					**Classification of Configuration:** ***Single* pack N** ***Dual* pack M** ***Six* in pack B** ***Chopper* Type L**
			1200				**Indication of rated current: 1200: I_C =1200 Amperes**
				GS			**Development Code: Type GS or JS: Third Generation Type GR: Fourth Generation Type C or D: High-Power**
					12		**Indication of rated V_{CES} (in Volts x 100)**
						AW	**Configuration of Characteristic Identification**

3.2 Internal Structure of Module

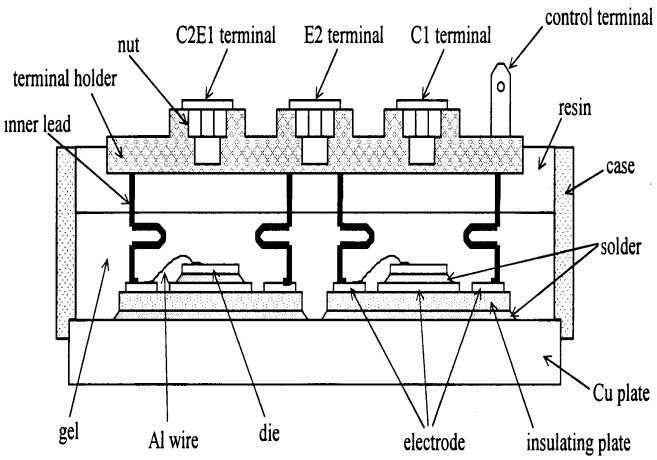


Figure 1. Dual Pack Module

Figure 1 shows a cross-sectional representation of the internal structure of an Hitachi IGBT module, specifically a dual-pack.

3.3 Internal Structure of an IGBT Die

Figure 2 shows the structure of punchthrough technology within an IGBT die.

An IGBT die is similar to an n-channel MOSFET in its structure. Although the MOSFET is constituted of N-N base, the IGBT is P-N base, so the parasitic pnp transistor is formed by an additional P layer.

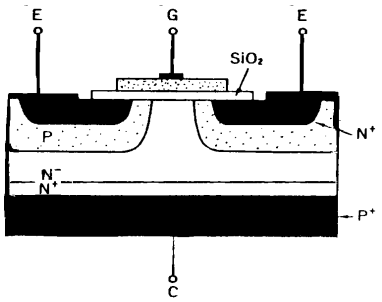


Figure 2. Structure of IGBT die

Definitions:

C	Collector
E	Emitter
G	Gate

3.4 Symbol and Equivalent Circuit

An IGBT module is essentially a switching transistor controlled by the voltage applied to its gate terminal. Figure 3 shows the symbol and equivalent circuit of an IGBT module.

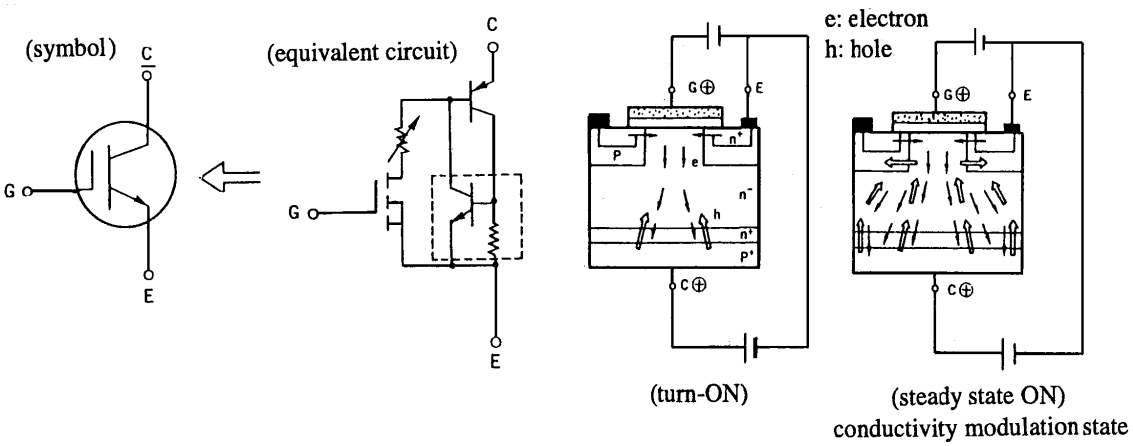


Figure 3. IGBT Symbol and Equivalent Circuit

3.5 Operational Switching Description

For IGBT turn-ON, the N-channel MOSFET is turned ON by first applying a positive voltage to gate-emitter electrode (see Figure 3). As a consequence, all of the MOSFET's drain current flows as the base current of the pnp transistor, so this transistor turns ON and the IGBT reaches its ON state.

For IGBT turn-OFF, a zero or minus bias must be applied as the gate-emitter voltage so that the MOSFET's current and the base current of the transistor will be cut off, thus causing the IGBT to reach an OFF state.

Note: ***Since an IGBT is comprised of MOSFET and pnp transistor structures, it is inherently able to reduce its ON state conduction loss, due mainly to the phenomenon of conductivity modulation.***

4 Specification and Characteristics

4.1 Contents of Specification

4.1.1 Absolute Maximum Ratings

Absolute maximum ratings apply to electrical, mechanical and thermal conditions that must be adhered to in order to prevent IGBT module destruction. Such conditions are generally expressed in terms of the maximum or minimum parameter values or to regions of Safe Operating Area (SOA).

4.1.2 Electrical Characteristics

The electrical characteristics for proper IGBT module functioning are maximum, typical, and minimum values expressed mainly in terms of steady-state, dynamic, and thermal characteristics.

4.1.3 Outline Drawing for IGBT Modules

An outline drawing provides the user with important information regarding an IGBT module's dimensions for proper setting to a heat sink, as well as the proper wiring of the IGBT module.

Figure 4 shows one such example of a typical outline drawing.

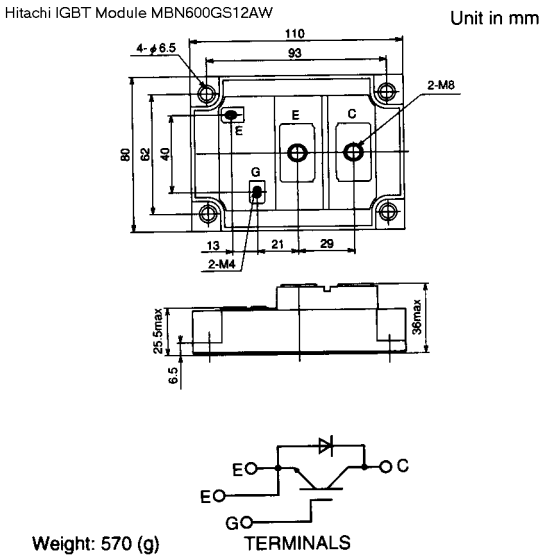


Figure 4. Typical IGBT Module Outline Drawing

4.1.4 Ratings and Characteristics

Figure 5 shows an example of the ratings and characteristics for a typical Hitachi IGBT module.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C)

Item		Symbol	Unit	MBN600GS12AW
Collector-Emitter Voltage		V_{CES}	V	1,200
Gate-Emitter Voltage		V_{GES}	V	±20
Collector Current	DC	I_C	A	600
	1 ms	I_{CP}		1,200
Forward Current	DC	I_F	A	600 (1)
	1 ms	I_{FM}		1,200
Collector Power Dissipation		P_c	W	3,100
Junction Temperature		T_j	°C	−40 ~ +150
Storage Temperature		T_{stg}	°C	−40 ~ +125
Isolation Voltage		—	V_{RMS}	2,500 (AC, 1 minute)
Screw Torque	Terminals	—	N·m	1.37(14)/7.84(80) (2)
	Mounting		(kgf·cm)	2.94 (30) (3)

Notes: (1) RMS Current of Diode 180 A rms
(2) Recommended Value 1.18/7.35 N·m (12/75 kgf·cm)
(3) Recommended Value 2.45 N·m (25 kgf·cm)

CHARACTERISTICS (T_C = 25°C)

Item		Symbol	Unit	Min.	Typ.	Max.	Test Conditions
Collector-Emitter Cut-Off Current		I_{CES}	mA	—	—	1.0	V_{CE} = 1,200V, V_{GE} = 0V
Gate-Emitter Leakage Current		I_{GES}	nA	—	—	±500	V_{GE} = ±20V, V_{CE} = 0V
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	V	—	2.7	3.4	I_C=600A, V_{GE} =15V
Gate-Emitter Threshold Voltage		$V_{GE(TO)}$	V	—	—	10	V_{CE} =5V, I_C =600mA
Input Capacitance		C_{ies}	pF	—	56,000	—	V_{CE} =10V, V_{GE}=0V, f =1MHz
Switching Times	Rise Time	t_r	μs	—	0.25	0.5	V_{CC} =600V
	Turn-ON Time	t_{on}		—	0.4	0.8	R_L =1.0Ω
	Fall Time	t_f		—	0.3	0.4	R_G=2.2Ω (4)
	Turn-OFF Time	t_{off}		—	0.8	1.2	V_{GE} =±15V
Peak Forward Voltage Drop		V_{FM}	V	—	2.5	3.5	I_F=600A, V_{GE}=0V
Reverse Recovery Time		t_{rr}	μs	—	—	0.4	I_F=600A, V_{GE}=−10V, di/dt=600A/μs
Thermal Impedance	IGBT	$R_{th(j-c)}$	°C/W	—	—	0.04	Junction to case
	FWD	$R_{th(j-c)}$		—	—	0.1	

Notes: (4) R_G value is the test condition's value for establishing switching times, not a recommended value.
Determine a suitable R_G value after measurement of switching waveforms (overshoot voltage, etc.) with appliance mounted.

Figure 5. IGBT Module Ratings and Characteristics

4.2 Characteristic Curves

4.2.1 Collector Current vs. Collector-Emitter Voltage

Figure 6 shows the relation between V_{CE} and I_C as a function of the gate-emitter voltage. This information is used to calculate the power loss of an IGBT's ON state.

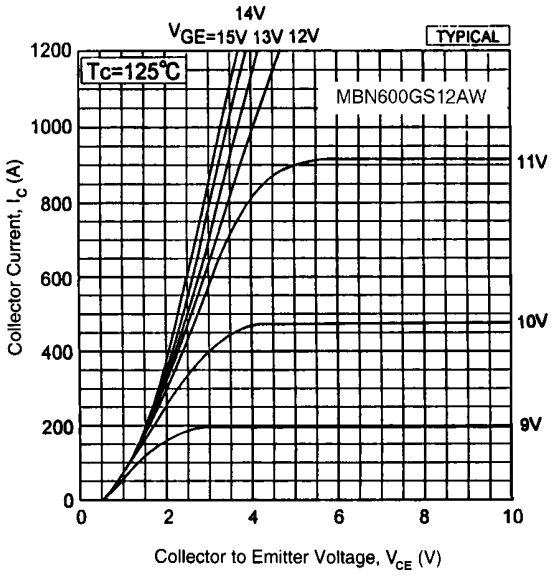


Figure 6. Collector Current vs. Collector-Emitter Voltage

4.2.2 Collector-Emitter Voltage vs. Gate-Emitter Voltage

Figure 7 shows a relation between V_{CE} and V_{GE} as a function of the collector current and including the V_{GE} area suitable for operating an IGBT. Generally, V_{GE} = 15 V.

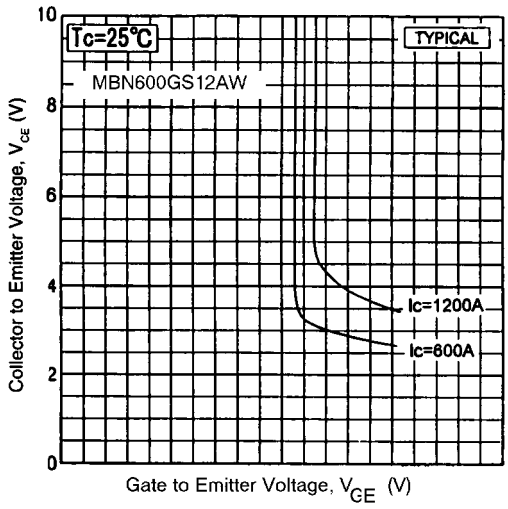


Figure 7. Collector-Emitter Voltage vs. Gate-Emitter Voltage

4.2.3 Gate Charge Characteristics

Figure 8 shows the relation between gate charge (Q_G) and gate-emitter voltage (V_{GE}), relating what amount of electric charge is required to operate an IGBT, how to determine the power supply capacitance at the output of a gate driver circuit, and how this information can be used to calculate the switching time.

Note: Refer to comments in section 5.7 concerning dead time.

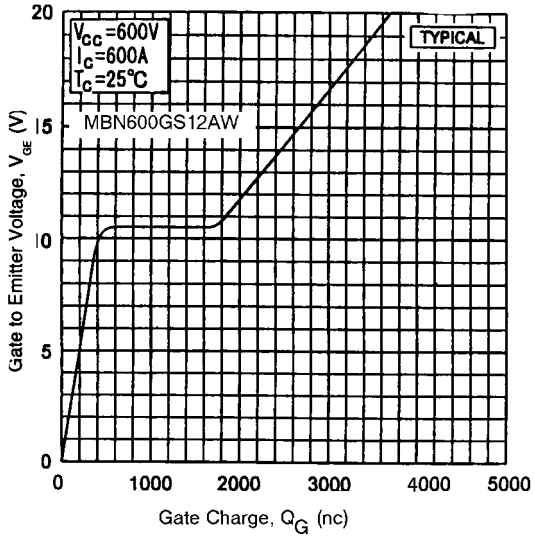


Figure 8. Gate Charge Characteristics

4.2.4 Forward Voltage Characteristics of a Free-Wheeling Diode

Figure 9 shows the forward voltage characteristics of a Free-Wheeling Diode (FWD). Such information can be used for calculating power loss associated with the diode's ON state.

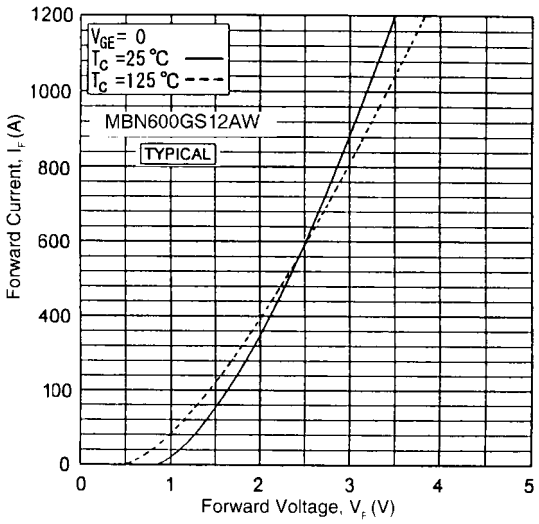


Figure 9. Forward Voltage Characteristics of a Free-Wheeling Diode

4.2.5 Switching Time vs. Collector Current

Figure 10 shows the turn-ON and turn-OFF switching times of an IGBT as a function of collector current (I_C). This information can be used to verify the influence of collector current upon switching time, especially for the setup of the device's dead time.

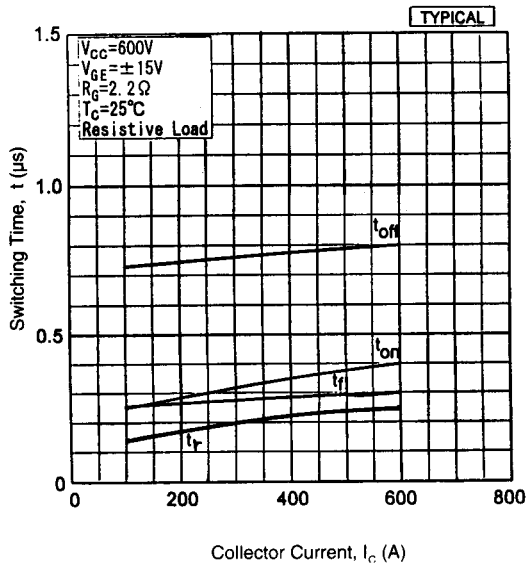


Figure 10. Switching Time vs. Collector Current

4.2.6 Switching Time vs. Gate Resistance

Figure 11 shows the turn-ON and turn-OFF switching times of an IGBT module as a function of gate resistance. (Refer also to section 4.2.5.)

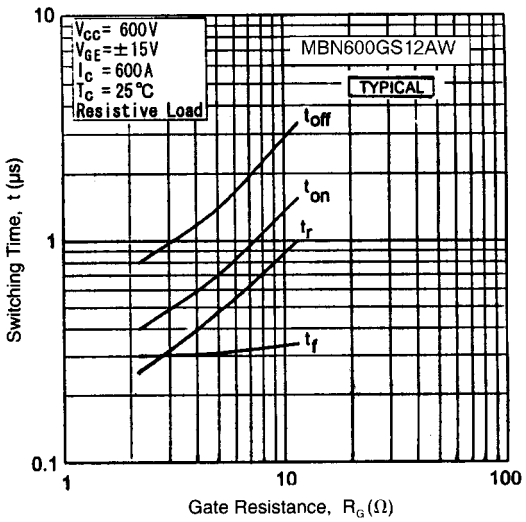


Figure 11. Switching Time vs. Gate Resistance

4.2.7 Switching Loss vs. Collector Current

Figure 12 shows the power loss dependency upon collector current during IGBT module turn-ON and turn-OFF. The information in this figure can be used for calculation of switching loss, that is, per single pulse at the inductive load switching circuit. So, loss can be calculated in terms of switching frequency.

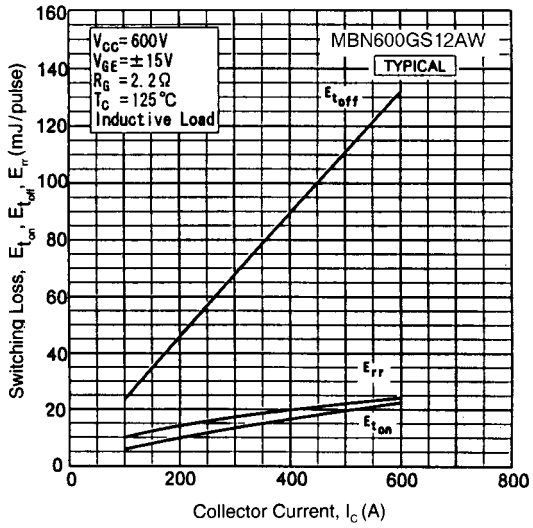


Figure 12. Switching Loss vs. Collector Current

4.2.8 Switching Loss vs. Gate Resistance

Figure 13 shows the power loss dependency upon R_G during IGBT turn-ON and turn-OFF. (Refer also to section 4.2.7).

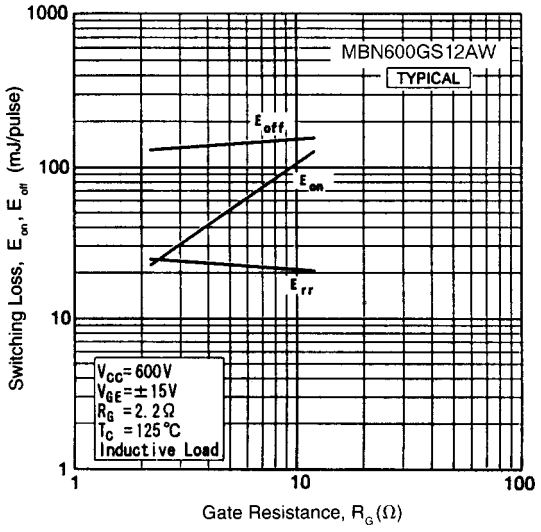


Figure 13. Switching Loss vs. Gate Resistance

4.2.9 Reverse-Biased Safe Operating Area

IGBT module-based applications must be designed to assure that both V_{CE} and I_C are within the safe operating area. Figure 14 shows one particular example of the permissible Reverse-Biased Safe Operating Area (RBSOA) of V_{CE} and I_C during IGBT turn-OFF.

Note: The value for V_{CE} includes the overshoot voltage.

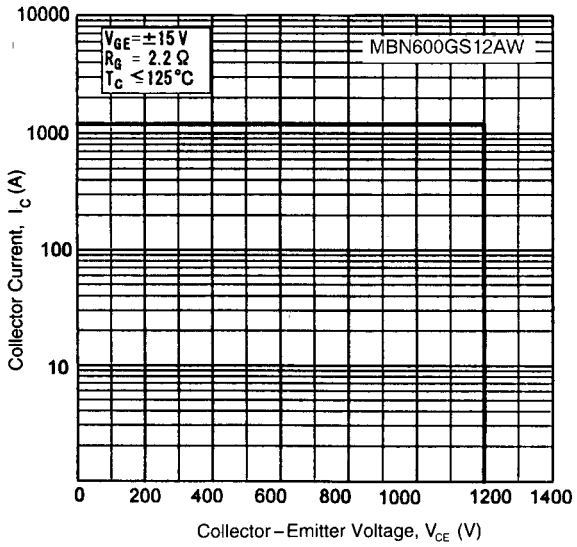


Figure 14. Reverse-Biased Safe Operating Area

4.2.10 Transient Thermal Impedance

Figure 15 shows transient thermal impedance characteristics for IGBT modules and diode devices.

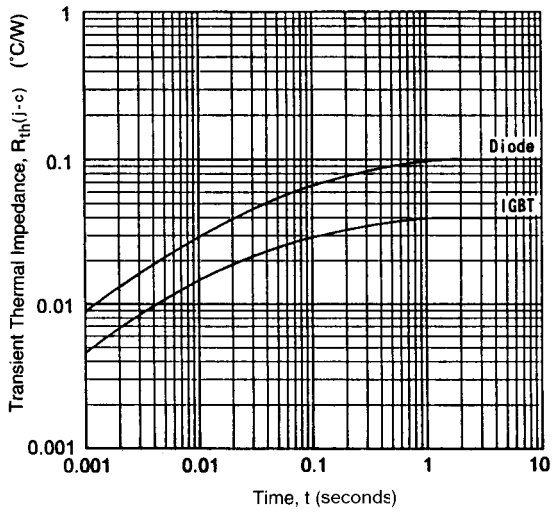


Figure 15. Transient Thermal Impedance Characteristics

4.3 IGBT Terms, Symbols, and Definitions

Table 2. IGBT Terms, Symbols, and Definitions

TERMS	SYMBOLS	DEFINITIONS
Collector-Emitter Voltage	V_{CES}	Maximum allowable collector-emitter voltage at shorted gate.
Gate-Emitter Voltage	V_{GES}	Maximum allowable gate-emitter voltage at shorted collector.
Collector Current	I_C	Within allowable collector power dissipation, maximum allowable value of DC current to collector terminal.
Collector Power Dissipation	P_C	Under specified heat conditions, maximum allowable value of constant collector power dissipation.
Junction Temperature	T_J	Range of allowable temperature at junction as basis of ratings.
Storage Temperature	T_{stg}	Range of allowable temperature for storage of IGBT module.
Screw Torque	- Maximum allowable value of clamping torque when IGBT module is mounted onto heat sink or support, using specified grease on screw and contact portions. - Maximum allowable clamping torque when wiring or bus is mounted to IGBT module terminals.	
Collector-Emitter Cut-Off Current	I_{CES}	Under specified conditions, collector current for applying collector-emitter voltage in cut-off state. **Note: Collector-emitter terminals are shorted.**
Gate-Emitter Leakage Current	I_{GES}	Under specified conditions, collector current for applying collector-emitter voltage in cut-off state. **Note: Collector-emitter terminals are shorted.**
Collector-Emitter Saturation Voltage	V_{CE} **(sat)**	Under specified conditions, value of saturation voltage when collector current is conducting.
Gate-Emitter Threshold	V_{GE} **(TO)**	Under specified conditions, value of gate-emitter voltage when collector current starts to flow (in threshold region).
Input Capacitance	C_{ies}	Under specified conditions, value of capacitance between gate and emitter terminals.
Reverse Transfer Capacitance	C_{res}	Under specified conditions, value of capacitance between gate and collector terminals.
Output Capacitance	C_{oes}	Under specified conditions, value of capacitance between collector and emitter terminals.
Turn-ON Time	t_{on}	Under specified conditions, time required for collector-emitter voltage to reach 10% of its initial value after the moment when ON-gate voltage has reached 10% of its final value and through the subsequent switching of IGBT module from OFF state to ON state ($t_d(on) + t_r$).
Turn-ON Delay Time	t_d **(on)**	Time required for collector-emitter voltage to reach 90% of its initial value after the moment when ON gate voltage has reached 10% of its final value.
Rise Time	t_r	Time required for collector-emitter voltage to reach 10% from 90% of its initial value.
Turn-OFF Time	t_{off}	Under specified conditions, time required for collector current to reach 10% of its initial value after the moment when OFF-gate voltage has reached 90% of its initial value and through the subsequent switching of IGBT module from ON state to OFF state ($t_d(off) + t_r$).
Turn-OFF Delay Time	t_d **(off)**	Time required for collector-emitter voltage to reach 90% of its initial value after the moment when OFF-gate voltage has reached 90% of its initial value.
Fall Time	t_f	Time required for collector current to reach 10% from 90% of its initial value.
Thermal Impedance	R_{th} **(j-c)**	Under thermal steady-state while IGBT module is continuously energized, value of temperature difference between junction and case per unit power dissipation at junction. Unit is $^oC/W$.
Reverse Recovery Time (Free-wheeling diode)	t_{rr}	Maximum allowable continuous peak current in forward direction of free-wheeling diode under specified circuit and temperature conditions.
Forward Current (Free-wheeling diode)	I_F	Maximum allowable continuous peak current in forward direction of free-wheeling diode under specified conditions.
Peak Forward Voltage Drop (Free-wheeling diode)	V_{FM}	Maximum instantaneous value of voltage drop between anode and cathode of free-wheeling diode under specified conditions of forward current (I_F) and temperature.

4.3.1 Measurement of IGBT Switching Characteristics

Figure 16 shows how switching characteristics for IGBT modules are measured.

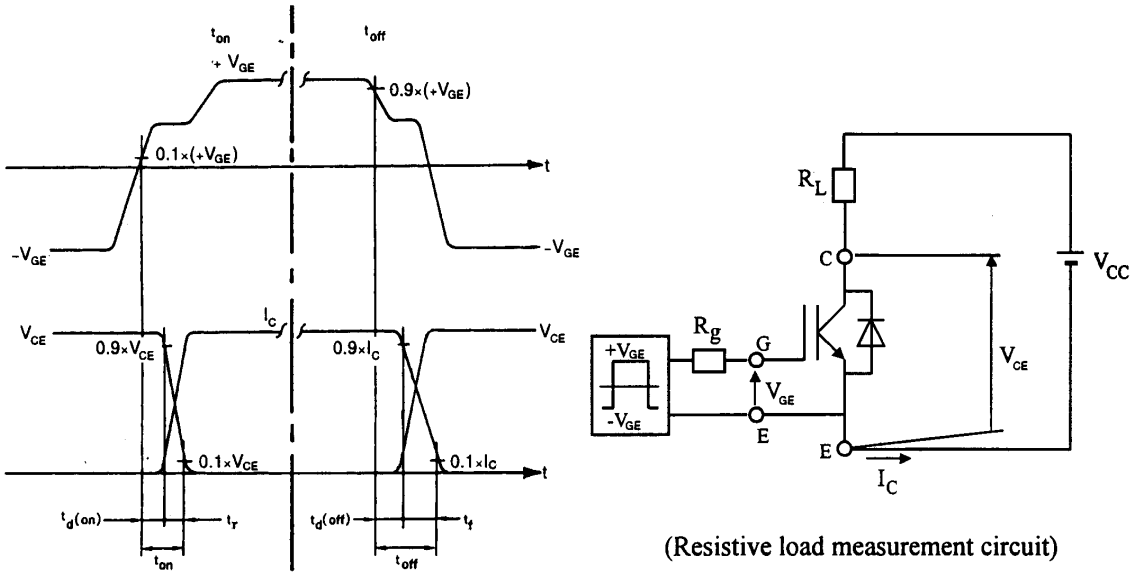


Figure 16. IGBT Switching Characteristics

4.3.2 Measurement of FWD Reverse-Recovery Characteristics

Figure 17 shows how reverse-recovery characteristics for Free-Wheeling Diodes are measured.

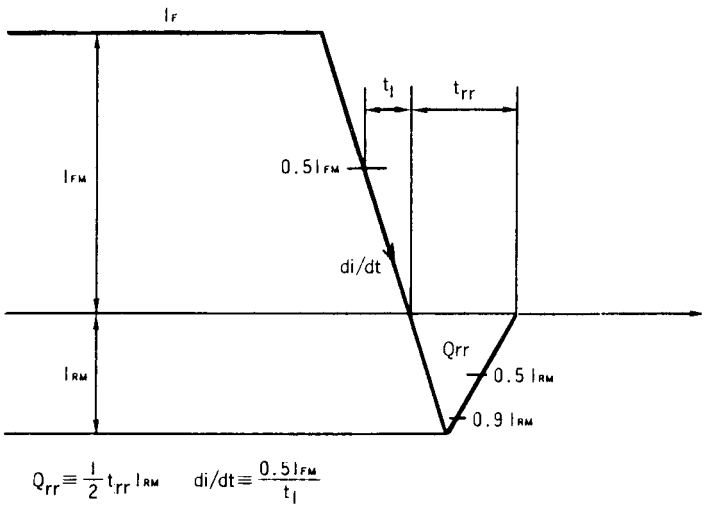


Figure 17. FWD Reverse-recovery Characteristics

5 Operating Parameters

5.1 Derating Factors

To ensure IGBT module reliability, follow each of the derating factors listed below.

5.1.1 Voltage

Maximum peak voltage should not exceed 80% of the rated voltage V_{CES}, and the DC voltage should not exceed 50 to 60% of V_{CES}.

Note: ***Use Equation 1 to calculate the rated voltage of an IGBT module for a given AC line input voltage at the inverter.***

Equation 1: $V_{CES} = V_{in} \sqrt{2} + V_s + V_{reg} + \alpha$

Definitions:

V_{CES}	Rated voltage of IGBT module
V_{in}	Input voltage of AC line
V_s	Overshoot voltage
V_{reg}	Increased voltage dependence on regeneration
α	Margin

5.1.2 Current

Maximum repetitive current peak value I_p should not exceed 70 to 80% of the rated DC current I_C.

Because faults, such as load short circuit, are taken into account for the one millisecond rated current I_{cp}, this value cannot be used repeatedly.

Note: ***Use Equation 2 to calculate the rated current of an IGBT module based on the peak current of the inverter.***

Equation 2: $I_p = P_{inv} \times \kappa \div V_{ac} / \sqrt{3} \times \sqrt{2} \times \lambda$

Definitions:

I_p	Peak current of inverter
P_{inv} (VA)	Inverter capacitance (equals motor capacitance divided by efficiency)
κ	Overload factor
V_{ac} (V_{rms})	AC voltage
λ	Ripple factor

5.1.3 Temperature

To use the overload of the motor, case temperatures should not exceed 100 ^{o}C, and the junction temperature should be no more than 70 to 80% of the rated maximum.

5.2 Snubber Circuit

Generally, snubber circuits are used to protect the switching IGBT module (when an IGBT module is turned OFF) by reducing the overshoot voltage generated by the charged energy in the line inductance. Actual monitoring of the turn-ON and turn-OFF switching waveform is always the best means for deciding what snubber circuit conditions exist and how to address them.

Note: ***For review and reference purposes, the following information regarding snubber circuits is included here.***

5.2.1 Features of Various Snubber Circuits

Figures 18 through 20 provide examples of three typical snubber circuits and their respective features.

5.2.1.1 Snubber Circuit between P and N

In Figure 18 the supply voltage is always charged in capacitor C_s and controls the overshoot voltage. Upper- or lower-side relations between D_s, R_s, and C_s are free, so this type of circuit is utilized for small capacity situations.

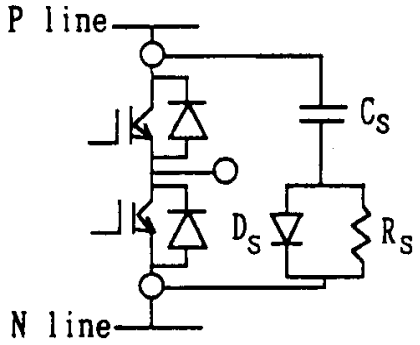


Figure 18. Snubber Circuit between P and N

5.2.1.2 Pair of Snubber Circuits between P and N

In Figure 19 the supply voltage is always charged in both capacitors (C_s) and controls the overshoot voltage at each arm. This type of circuit is utilized for large capacity situations.

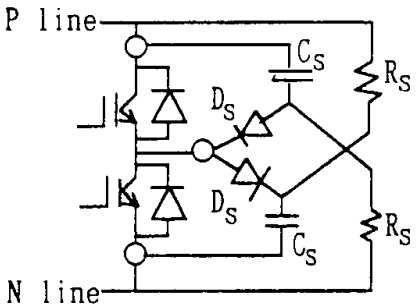


Figure 19. Pair of Snubber Circuits between P and N

5.2.1.3 Pair of Snubber Circuits between Arms

In Figure 20 charge and discharge are repeated on every switching of each arm from 0V to supply voltage. Because the snubber loss is large, this circuit is best suited to narrow Reverse-Biased Safe Operating Area (RBSOA) devices and would, generally, not be used with IGBT modules.

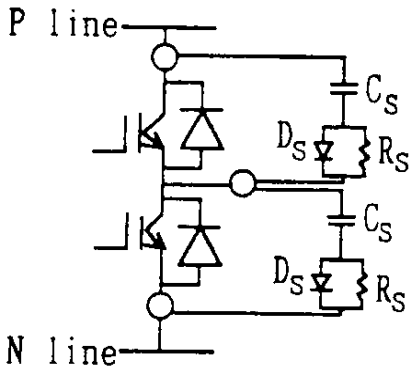


Figure 20. Pair of Snubber Circuits between Arms

5.2.2 Snubber Circuit Operation

Figure 21 represents a circuit in the overvoltage occurrence mode of a bottom-arm IGBT at the time of turning OFF. Figure 22 represents an equivalent circuit in a transient state at the same time.

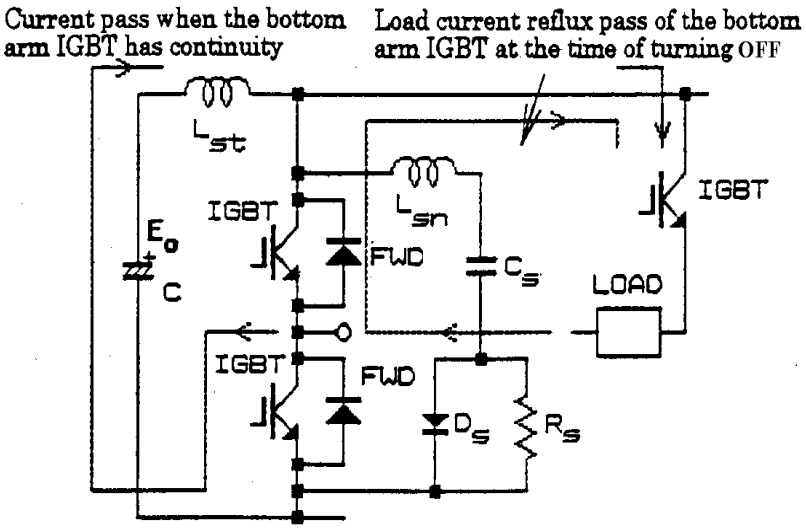


Figure 21. Turn-OFF Mode of bottom arm IGBT

Figure 21 represents changes in the current pass when the bottom IGBT, which was ON, is turned OFF. When the bottom arm IGBT is turned OFF, the load current passes through the FWD at the top arm and is refluxed. Discharge of energy accumulated in the L_{st} is applied to the bottom arm IGBT as an overvoltage because the absence of a snubber circuit results in the loss of a discharge destination.

Figure 22 shows that installing a snubber circuit results in L_{st} energy passing through the snubber circuit and being refluxed. This allows overvoltage suppression. However, in reality, the snubber circuit also has wiring inductance L_{sn} which may cause overvoltages. How can L_{st} and L_{sn} be reduced? The answer is to choose the right components and to lay them out appropriately.

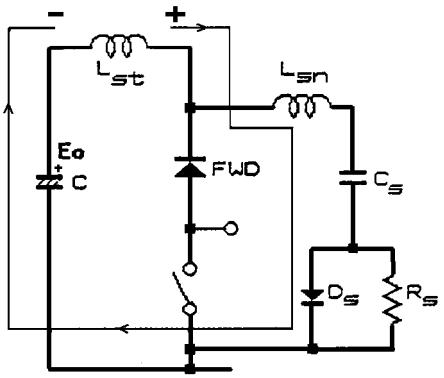


Figure 22. Equivalent Circuit (transient state)

5.2.3 Snubber Circuit Current and Voltage Waveforms

Referring to Figure 21 above, consider the current and voltage waveforms in the circuit when the IGBT is turned OFF. Figure 23 represents the IGBT module's turn-OFF current and voltage waveforms and clearly shows that use of a snubber circuit inhibits surge voltage stemming from wiring inductance L_{st} to $E_o + \Delta V_f$.

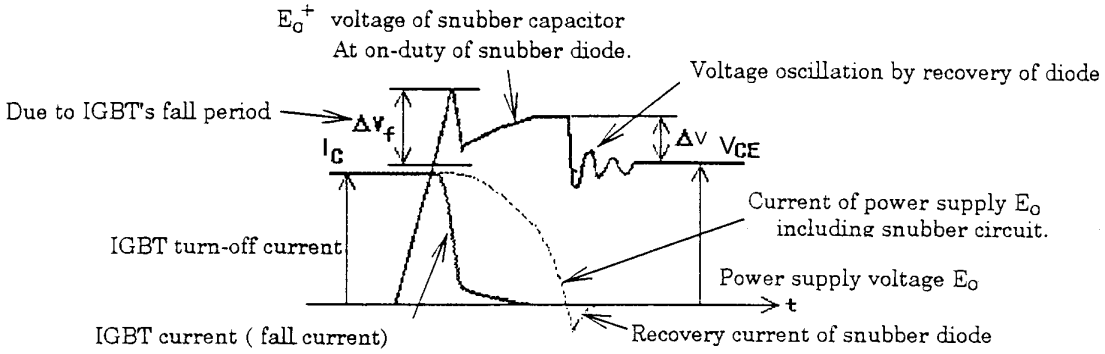


Figure 23. IGBT Module Current and Voltage Waveforms with Snubber Circuit

Figure 24 shows current and voltage waveforms of the snubber diode D_S when the snubber circuit functions.

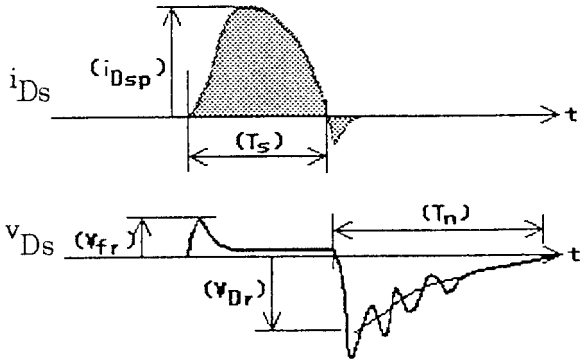


Figure 24. Snubber Diode Current and Voltage Waveforms

Values associated with the labeled portions of Figures 23 and 24 can be determined using Equations 3, 4, 5, and 6:

Equation 3: $T_S = 2\pi \times (\sqrt{LstxCs})/4$

Equation 4: $\Delta V = I_C \times \sqrt{\frac{(Lst)}{Cs}}$

Equation 5: $\Delta V_f = L_{sn} \times di_c/dt + V_{fr}$

Definitions:

I_C	IGBT turn-OFF current
L_{sn}	Snubber circuit inductance as viewed from IGBT's collector and emitter terminals
V_{fr}	Forward recovery voltage (typically about 50V)
di_c/dt	Current change ratio in IGBT's fall period.

In addition, the value for T_n which is defined as the time required to discharge 95% of the overcharge voltage of C_s is approximated using Equation 6:

Equation 6: $T_n = 3 \times C_s \times R_s$

Here, R_s must be set to a value such that $T_S + T_n < 1/f_c$.

Note: ***In the above equation, for the case of a three-phase circuit, the value for T_S in Equation 3 must be multiplied by $\sqrt{3}$, and the ΔV in Equation 4 must be multiplied by $1/\sqrt{3}$.***

5.2.4 Collector Current Class and Snubber Capacitor Values

The snubber circuit capacitor value can be calculated using Equation 7:

Equation 7: $C = L_{st}(I/\Delta V)^2$

Table 3 gives approximate guidelines for snubber capacitor values.

Table 3. Snubber Capacitor Values

Rated Collector Current (I_C)	Snubber Capacitor Values (μF)
50 A class	0.10 to 0.22
75 A class	0.15 to 0.33
100 A class	0.22 to 0.68
150 A class	0.33 to 1.00
200 A class	0.47 to 1.50
300 A class	0.68 to 2.20
400 A class	1.00 to 3.30
600 A class	2.20 to 4.70

Depending on the inductance of the main circuit wiring, larger capacitance values than are listed in Table 3 may be required. For a snubber capacitor, use a polyester film capacitor or an oil capacitor with good frequency characteristics.

5.2.5 Snubber Resistance Selection

The resistor value varies according to capacitor value and the IGBT's driving frequency. When voltage ΔV overcharged to the snubber is used, εS_n generated when the current I is turned OFF becomes, according to Equation 8:

Equation 8: $$\varepsilon S_n = 0.5 \times C_S \times (\Delta V)^2$$

Most of this energy can be considered to be consumed by snubber resistance. Supposing that the output current of a voltage inverter or something similar is a sinusoidal current with current I in Equation 7 as a peak value, the energy of the snubber circuit can be considered to occur as a sine wave with εS_n in Equation 8 as a peak value. The average generated loss P_{SN} in the P-N snubber circuit, taking into account the switching of the top and bottom arms becomes, according to Equation 9:

Equation 9: $$P_{SN} = (2/\pi) \times \varepsilon S_n \times f_c$$

where f_c is a switching frequency.

Equation 10 indicates what resistance value must be selected to prevent oscillation of the collector current at IGBT turn-ON.

Equation 10: $$R_S \geq 2\sqrt{\frac{(Lsn)}{Cs}}$$

where L_{sn} is the inductance of the snubber wiring.

Note: ***R_s represents resistance in discharging ΔV overcharged to C_s, so that the top limit must be noted.***

5.2.6 Snubber Diode Selection

Select a snubber diode having the same class as the IGBT's rated collector emitter voltage value. Use an IGBT module with a current rating of 1/10 to 1/5 that of the IGBT used.

5.3 Gate Driving Considerations

5.3.1 Gate Current and Gate Electric Charge

Figure 25 shows the waveform of current and voltage during IGBT module operation.

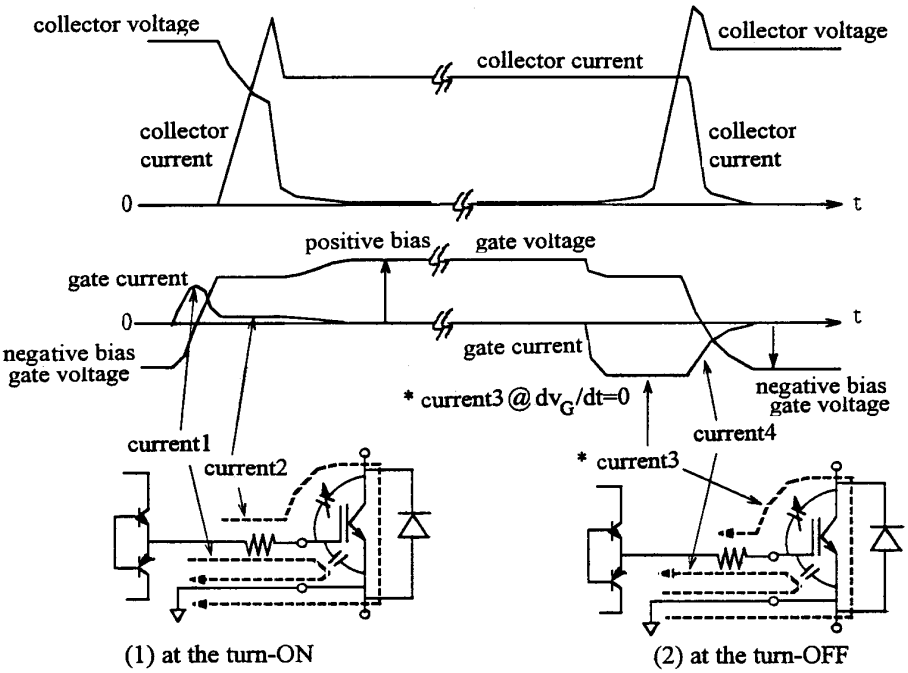


Figure 25. Example of IGBT switching waveform

During turn-ON and turn-OFF, the gate current necessary to charge and discharge input capacitance (C_{ies}) and reverse transfer capacitance (C_{res}) flows between gate- and emitter-controlling electrodes.

So, when gate-emitter voltage is applied to establish either positive or negative bias, the product of gate current and time represents the amount of gate electric charge transferred.

5.3.2 Gate Electric Charge Characteristics

Figure 26 shows the relation between gate electric charge (Q_G) and gate-emitter voltage and segments the gate electric charge characteristics into three regions (labeled A, B, and C).

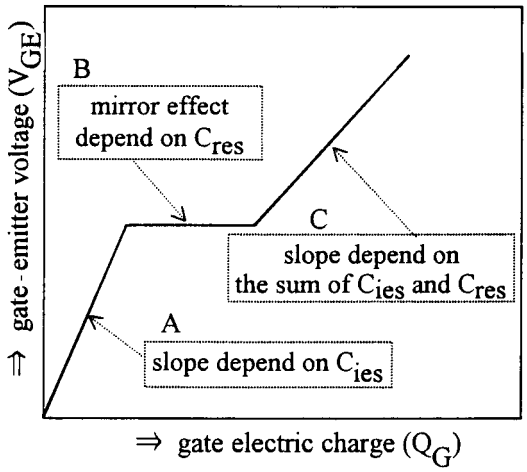


Figure 26. Example of Gate Electric Charge Characteristics

A: Region A clearly shows that the electric charge (Q_G) is determined by gate voltage and input capacitance of IGBT module during the condition that collector-emitter voltage is higher than the output voltage of the gate driver.

B: Region B shows the negative reverse transfer ("mirror effect") of reverse transfer capacitance (C_{res}). Here, gate-emitter voltage cannot vary, but collector-emitter voltage does and, as a consequence, gate current remains constant with value determined by the output voltage of the gate driver and gate resistance.

C: Region C shows the situation where the collector-emitter voltage approaches the saturation voltage while the input capacitance and maximum value of reverse transfer capacitance are connected in parallel.

5.3.3 Gate Driving Loss Calculation

Gate driver circuit power loss can be calculated from an examination of the gate electric charge characteristics. Figure 27 shows the gate electric charge characteristics (including the negative bias voltage area) where V_{GP} and V_{GN} are the positive and negative bias voltage values. Gate electric charge varies as the value of Q_{GO} depends on V_{GN} to V_{GP} transfer (that is, turn-ON) and V_{GP} to V_{GN} transfer (that is, turn-OFF). In this case, Equation 11 can be used to calculate the driver circuit (P_G) power (where f_c represents switching frequency).

Equation 11: $$P_G = (V_{GP} + V_{GN}) \times Q_{GO} \times f_c$$

Note: ***Driver circuit power for switching must be supplied by the driver circuit power supply and is directly proportional to the switching frequency. Remember to take this fact into account when designing the power supply circuit.***

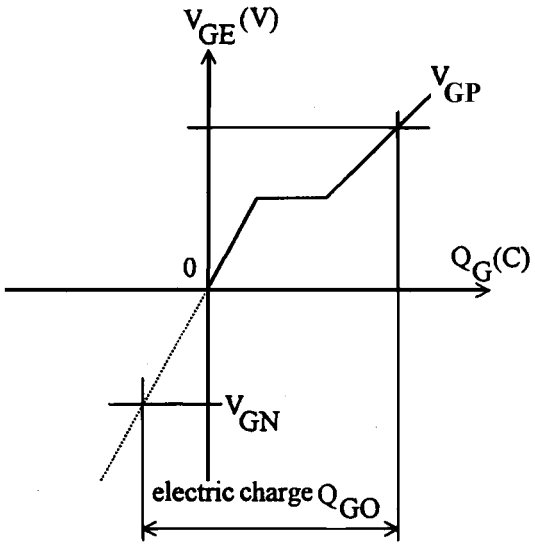


Figure 27. Driving Voltage and Gate Electric Charge

5.3.4 IGBT Driving Voltage

The IGBT driving voltage needs to set up both positive and negative bias voltages. Lower positive bias causes increased ON-state loss, and higher positive bias promotes increased short-circuit current. For these reasons, it is particularly important to always select an appropriate driving voltage.

Note: ***A positive bias of 15V ± 10% and a negative bias of from -5V to -15V are recommended to prevent misoperation when the other arm (device) switching occurs.***

5.4 Parallel Circuitry Connections

As described earlier in this document, punchthrough technology is used to produce Hitachi IGBT modules. However, because increased power handling solutions require special considerations, this section describes matters related to parallel circuit connections of IGBT modules.

5.4.1 V_{ce} (sat) Classify and Current Unbalanced Rate

Table 4 provides classification examples of collector-emitter saturation voltages associated with two rated V_{CE} values.

Table 4. Ranking of Collector-Emitter Saturation Voltages

(1) Rated V_{CE} = 600 V			(2) Rated V_{CE} = 1200 V	
Rank	**V_{CE} (sat) (V)**		**Rank**	**V_{ce} (sat) (V)**
1	1.6 to 1.9			
2	1.7 to 2.0			
3	1.8 to 2.1			
4	1.9 to 2.2			
5	2.0 to 2.3			
6	2.2 to 2.5			
			6	2.2 to 2.5
			7	2.3 to 2.6
			8	2.4 to 2.7
			9	2.5 to 2.8
			10	2.6 to 2.9
			11	2.7 to 3.0
			12	2.8 to 3.1
			13	2.9 to 3.2
			14	3.0 to 3.3
			15	3.1 to 3.4

The saturation voltage range (ΔV_{ce} (sat)) is 0.3 V, as above, and in this condition the current unbalanced rate (α) is 15% where the definition of α is as stated in Equation 12:

Equation 12: $\alpha = \{ I_c' / (I_{total} / 2) - 1 \} \times 100\ (\%)$

Definitions:

I_c' Current value per individual IGBT module

I_{total} Total current per parallel connection pair

5.4.2 Parallel Connections and Current Derating

Although there is no limitation to the number of IGBT modules that can be connected in parallel, the negative effect reflected in an increase in the line inductance for power supply connection, e.g. surge voltage, etc. must always be taken into account. Under worst-case conditions, that current is concentrated in one IGBT module, with the current derating (R) as expressed by Equation 13.

Equation 13: $R = \{1+(n-1) \times (1 - \alpha/100)/(1 + \alpha/100)\}/n \times 100$

Definitions:

n	Number of parallel connections
α	Current unbalanced rate (15%)

Example: For the case involving four (4) IGBT modules connected in parallel and having rated current of 400 A, the current derating value R equals 80.4%, resulting in a total current of 400 A × 4 parallel × 0.804 = 1286 Amps.

5.4.3 Parallel Connection Line Unbalancing Notes

When connecting IGBT's in parallel, always take into consideration the following two key points:

I) Minimize the difference in V_{CE} (sat) of the elements in order to prevent current unbalance during stable operation, and

II) Minimize line unbalancing when arranging the elements in parallel in order to minimize transient current unbalancing when the main circuit is either turned ON or OFF.

Although the difference among the elements, as stated under item I) above, can be reduced by the manufacturer via sorting and rank marking for V_{CE} , users must provide their own measures for item II).

As a general guideline, however, current unbalancing should be limited to a maximum of approximately 15%. Some possible measures that users should take to minimize line unbalancing are reviewed below.

5.4.3.1 Number of Drivers per Arm

To avoid adverse effects in parallel motion caused by deviations in delayed outputs from multiple drivers, use a one-driver arrangement that contains some signal processing circuit (photo-coupler, over-current protector, etc.) and connect all the drive elements in parallel.

5.4.3.2 Buffer Circuit for the Driver

In general, a buffer circuit is required for the driver to drive the elements connected in parallel. For this particular case, a buffer circuit design is shown in Figure 28 (with some of the parts omitted) along with a list of recommended transistors (see Table 5). Here, transistors Q1 and Q2 should be a complementary pair.

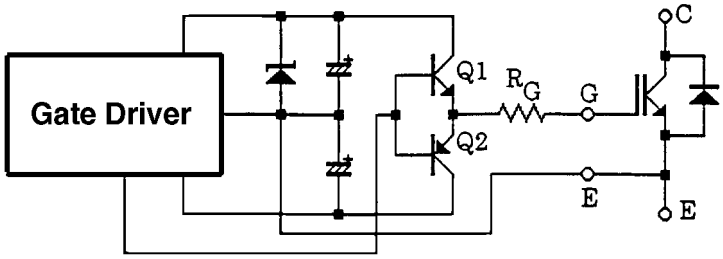


Figure 28. Driver Buffer Circuit (partial)

Table 5. Recommended Transistors

	I_C	Type	Model Numbers for Q1 and Q2
1	5A	NPN	2SD1722 (50V)
	5A	PNP	2SD1165 (-50V)
2	8A	NPN	2SD1723 (50V)
	8A	PNP	2SD1166 (-50V)

Note: ***Buffer transistors Q1 and Q2 need to be selected based on the desired output current level of the driver.***

5.4.3.3 Connecting Gate Resistors in Parallel Circuits

Figure 29 shows a recommended arrangement to connect the gate resistor to the parallel circuit to minimize gate voltage variation due to mutual interference among the respective modules. In addition, attention needs to be paid to the following points when using this particular configuration:

- Make use of twisted pair cable for the driver output line to minimize line impedance.
- Have the same inductance (L_{gst}) in each line loop (A and B) and minimize its value as much as possible.

  Note: ***The objective of the recommendations described under items I) and II) in section 5.4.3 is to avoid giving adverse effect due to inductance created when the main circuit is switched ON or OFF.***

- Recognize the fact that the gate voltage variation stated above occurs when the main circuit is either turned ON or OFF. To avoid the variation, maintain the relationship between the gate resistor (R_G) and loop inductance (L_{gst}) which can satisfy Equation 14.

Equation 14: $$2R_G > 2\,(L_{gst})/(C_{ies} / 2))^{1/2}$$

where C_{ies} represents the gate input capacitance of the IGBT.

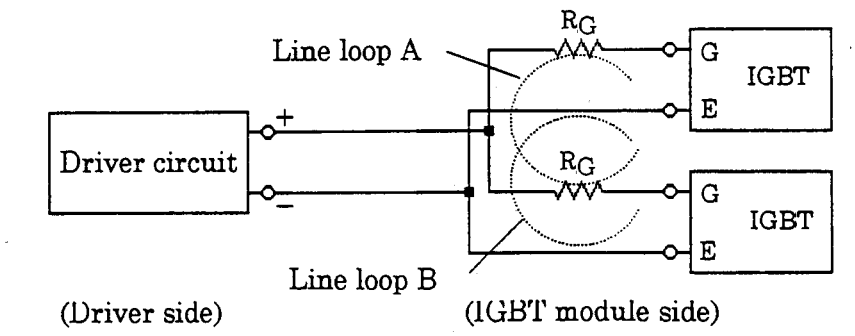


Figure 29. Parallel Connection between IGBT Modules and Driver Circuit

5.4.3.4 Necessity for Symmetry of Main Circuit Wiring

5.4.3.4.1 Wiring Equalization

For IGBT modules to be connected in parallel, it is essential to equalize the wiring on the collector and the wiring on the emitter with each other to keep inductance values in balance.

Figure 30 represents an example of double-parallel wiring and shows a schematic diagram of a parallel circuit including main circuit wiring inductance circuits.

For the collector, wiring inductance circuits L_{CA} and L_{CB} are shown, and for the emitter, wiring inductance circuits L_{EA} and L_{EB}.

When IGBTs (A) and (B) are turning ON, the current generated on each individual collector depends on the variations of the inductance circuits rather than on each element's characteristics.

Because the current balance depends principally on the inductance ratio, it is important to keep symmetry in wiring by matching the inductance values. For example, referring to Figure 30, if L_{CA} and L_{CB} are unbalanced (that is, $L_{CA} > L_{CB}$) and the V_{CE} (sat) value of IGBT (A) is smaller, then the current sharing as depicted in Figure 31 will result. In particular, if emitter lines L_{EA} and L_{EB} are unbalanced, the IGBT gate voltage will be adversely influenced, causing an unbalanced current.

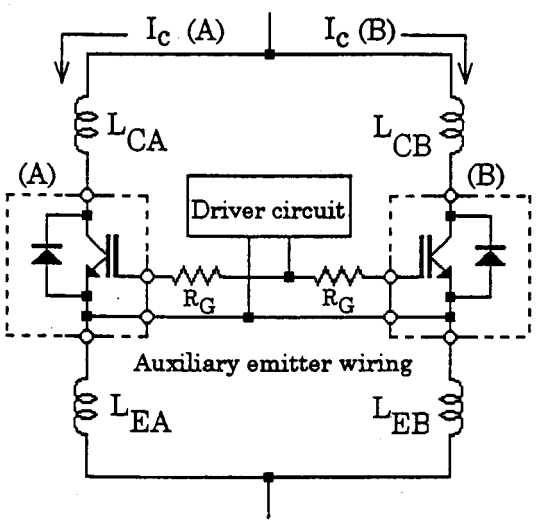


Figure 30. Wiring to equalize main wiring inductance values

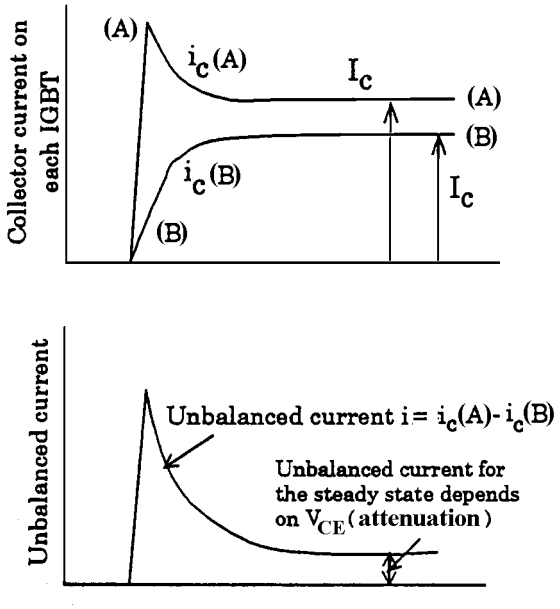


Figure 31. Equalization of Unbalanced Current

5.4.3.4.2 Unbalanced Current Period caused by Wiring

Figure 31 shows that once a current imbalance occurs when turning ON an IGBT, it will be equalized during the steady-state condition after activating the IGBT, finally settling down to values I_{CA} and I_{CB} as determined by V_{CE} (sat).

The time required for the unbalanced current to be equalized can be calculated as the attenuation over the L - R circuit caused by the inductance within the closed-loop forming a parallel circuit and the operating resistance of the IGBT element. The operating resistance " r_{on} " can be easily calculated from the output characteristics curve. For example, for an MBN300GS12AW IGBT module having a single arm, an " r_{on} " of approximately 4.2 milliohms (when T_j = 25 °C, 1/2 rated current) will be present. If the loop inductance is 100 nH for a parallel configuration, ($L_{CA} + L_{CB} + L_{EA} + L_{EB}$), the equalization in unbalanced current occurs based on the time constant τ is approximated by Equation 15.

Equation 15: $\tau = 100\,nH / (4.2\,m\Omega \times 2) \cong 12\,\mu s$

If the stability in the current variation is assumed to be three times τ (that is, variation is approximate, up to 95%), the current balance cannot be determined by V_{CE} (sat) within 36 μs after turning ON. This means if the carrier frequency is high or the active time is shorter, the current balance may be determined by the wiring (including the shape) for almost the whole period.

5.4.3.4.3 Wiring Example

Note: ***Although this example uses a 1-in-1 element, the results are the same for a 2-in-1 element.***

Figure 32 shows two parallels for a 1-in-1 module. The upper and lower arms are combined as a unit. The gate wiring must be configured orthogonally or separated to avoid mutual induction. To make the inductance of the gate wiring as small as possible, use a tightly twisted pair or similar wiring techniques. Figure 32 shows the main wiring using a copper bus bar. If the main circuit power supply capacitor corresponding to the number of parallels is arranged as shown in Figure 32, the current balance can easily be kept even with a hardware configuration using laminate bus bars (that is, a configuration that makes use of mutually insulated and cemented wiring plates P and N). Also, make sure that all output terminal wiring is balanced, and when using gate wiring in parallel, including this type, note the following:

i) To avoid noise generation in gate wiring or main circuit wiring due to mutual induction or excessive potential difference, use orthogonal wiring or keep adequate distance between cables. If you must use balanced wiring, maintain low inductance over the gate wiring.

ii) Since there is a high potential difference between the upper and lower arm gate wires, keep them sufficiently apart from each other.

iii) For the upper and lower arm gate wires, make equal the lengths and inductance values of the wires connecting to the drivers. (Use twisted pairs of the same length for the gate wires.)

Note: ***Connect a snubber circuit between segment C and E of each module to restrict the surge voltage.***

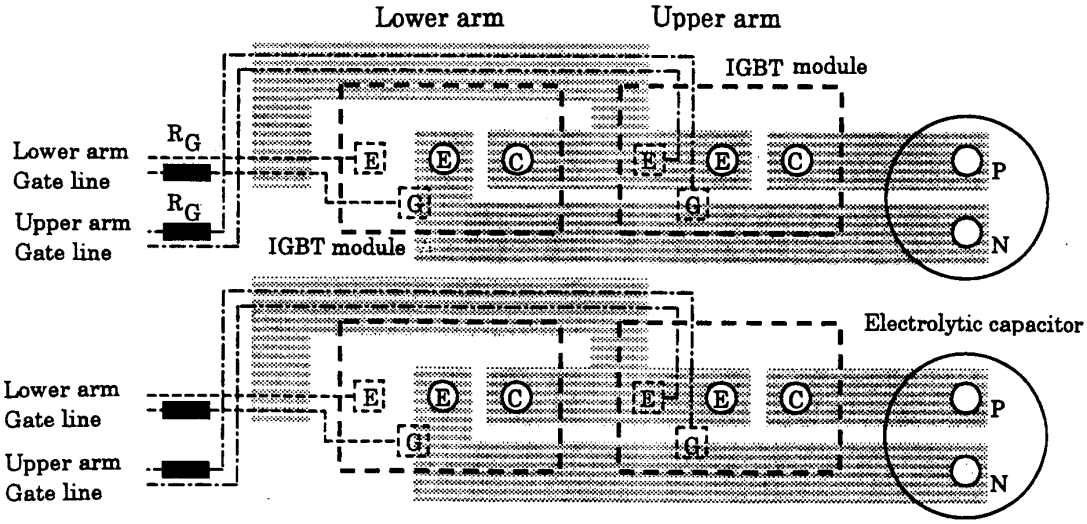


Figure 32. Example of Parallel Connection Wiring

5.5 Calculation of Power Dissipation

When an IGBT is used in a Variable-Voltage Variable-Frequency (VVVF) inverter circuit, a general calculation of power dissipation can be estimated as shown below.

Note:All calculations are based on a premise that the output is a sine wave.

5.5.1 Power Losses Occurring in Dual-Pack IGBT Modules

Total power dissipation = 2 × {Power dissipation in IGBT + Power dissipation in FWD}
IGBT power dissipation = Steady-state power dissipation (P_{on})
+ Turn-ON power dissipation (P_{ton})
+ Turn-OFF power dissipation (P_{toff})
FWD power dissipation = Forward power dissipation (P_f) + Recovery power dissipation (P_{rr})

5.5.1.1 IGBT Power Dissipation

5.5.1.1.1 Steady-state Power Dissipation

Equation 16: $P_{on} = 1/2\,\pi \int_0^{\pi} i\, v\, D\, dt$; (D: On-duty)

Equation 17: $D = (1 + \sin\Theta)/2$

A real control value $D = \kappa\,(1 + \sin\Theta)/2$ can be obtained by multiplying by the coefficient of on-duty. In this case, $\kappa = 1$ is supposed.

The steady-state power dissipation can be obtained using Equation 18:

Equation 18:

$$P_{on} = \{\sqrt{2}\, I_0/(2\pi)\} \times \{a + (\pi/4)\, b \times \sqrt{2}\, I_0 + (\pi/4) \times \cos\phi \times [a + (8b/(3\pi)) \times \sqrt{2}\, I_0]\}$$

Definitions:

i	Collector current flowing to IGBT (instantaneous value)
v	Saturation voltage (instantaneous value)
I_0	Inverter phase output current rms value (equal to the IGBT current)
a, b	Linear approximate curve value represented by $V_{CE}(sat) = a + bi$ (Obtain it from the I_C - V_{CE} characteristics shown in Figure 33)
cosϕ :	Load power factor

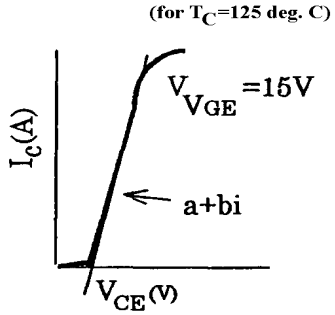


Figure 33. I_C vs. V_{CE} Characteristic

5.5.1.1.2 Turn-ON Power Dissipation and Turn-OFF Power Dissipation

Supposing that the inverter phase output current rms value is I_0, the output current peak value becomes $\sqrt{2}\, I_0$.

The average value of IGBT module turn-ON current and turn-OFF current is, according to Equation 19:

Equation 19: $I_{ave} = (2/\pi) \times \sqrt{2}\, I_0$

Obtain the turn-OFF power dissipation and the turn-ON power dissipation for the above I_{ave} (per pulse) and specify them as E_{ton} and E_{toff} (Figure 34), respectively.

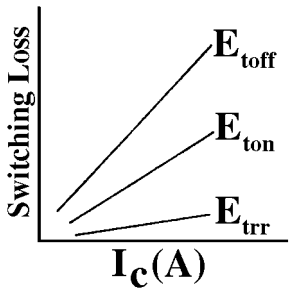


Figure 34. Switching Loss vs. Collector Current

Equations 20 and 21 can be used to calculate turn-ON power dissipation P_{ton} and turn-OFF power dissipation P_{toff} as a function of carrier frequency f_c.

Equation 20: $P_{ton} = E_{ton} \times f_c / 2$

Equation 21: $P_{toff} = E_{toff} \times f_c / 2$

5.5.1.2 Power Dissipation in a Free-Wheeling Diode

5.5.1.2.1 Forward Power Dissipation

Equation 22 provides a means for calculating forward power dissipation in a free-wheeling diode.

Equation 22:

$$P_f = (1/2\pi) \int_0^{\pi} \sqrt{2}\, I_0 \sin\theta \times (a + b\sqrt{2}\, I_0 \sin\theta) \times [\,(1 - \sin(\theta - \phi))/2\,]\, d\theta$$

$$= \{\sqrt{2}\, I_0 / (2\pi)\} \times \{a + (\pi/4)\, b \times \sqrt{2}\, I_0 - (\pi/4) \times \cos\theta \times [\,a + (8b/(3\pi)) \times \sqrt{2}\, I_0\,]\}$$

Definitions:

I_0	Inverter phase output current rms value
a, b	Linear approximate curve value represented by $V_f = a + bi$ (refer to Figure 35)
$\cos\phi$	Load power factor

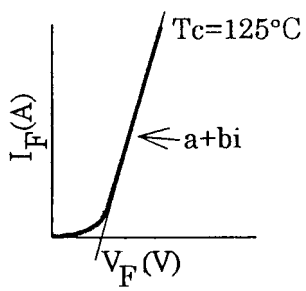


Figure 35. Forward Voltage Characteristics of Free-Wheeling Diode

5.5.1.2.2 Recovery Power Dissipation

Supposing that the current peak value is $\sqrt{2}\ I_0$, the forward average current (as calculated using Equation 23) becomes:

Equation 23: $I_{ave} = 2/\pi \times \sqrt{2}\ I_0$

For the above I_{ave} (per pulse), obtain the recovery power dissipation, specify it as E_{rr} (Figure 35), and then use Equation 24 to obtain the value for P_{rr}.

Equation 24: $P_{rr} = E_{rr} \times f_c / 2$

5.6 Thermal Impedance and Heat Dissipation Design

5.6.1 Thermal Impedance

Thermal impedance between junction and case (R_{th} (j - c)) of IGBT and diode is restricted in the device specifications.

*Note: **Thermal impedance values between case and heat sink (R_{th} (c - h)) of specific Hitachi IGBT modules can be supplied individually upon request.***

5.6.2 Definition of Temperature Measurement Point

Figure 36 shows that values for R_{th} (o - c) and R_{th} (c - h) are based on the indicated measurement points.

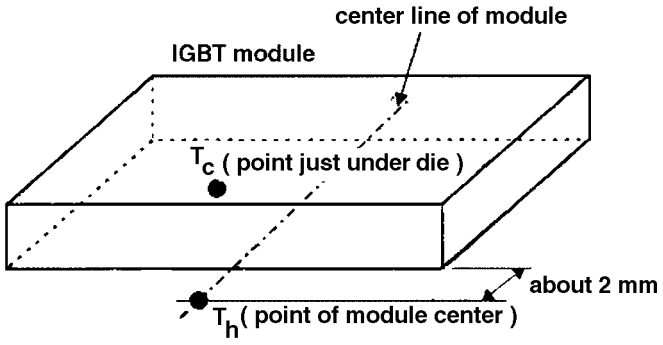


Figure 36. Definition of T_c and T_h Measurement Points

Legend:

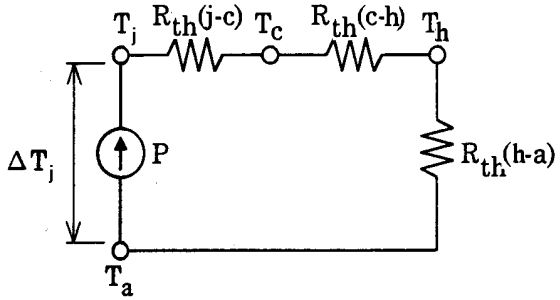
T_c	Case temperature of module
T_h	Heat sink temperature

5.6.3 Heat Dissipation Design

This section presents a basic procedure for selecting a heat sink based on steady state and transient state considerations.

5.6.3.1 Steady State

Figure 37 represents the thermal equivalent circuit and includes the parameter notations used in the equations which follow.



P Average power dissipation
T_j Junction temperature of dice
T_c Case temperature
T_h Heatsink temperature
T_a Air temperature
$R_{th}(j\text{-}c)$ Thermal impedance of junction to case
$R_{th}(c\text{-}h)$ Thermal impedance of case to heatsink
$R_{th}(h\text{-}a)$ Thermal impedance of heatsink to air

Figure 37. Thermal Equivalent Circuit

The junction temperature (T_j) can be estimated using Equation 25:

Equation 25: $$T_j = P \{ R_{th}(j\text{-}c) + R_{th}(c\text{-}h) + R_{th}(h\text{-}a) \} + T_a$$

Also, the change in junction temperature (ΔT_j) can be calculated using Equation 26:

Equation 26: $$\Delta T_j = P \times (R_{th}(j\text{-}c) + R_{th}(c\text{-}h) + R_{th}(h\text{-}a))$$

Here, the measurement points for T_c and T_h are as shown in Figure 36.

> ***Note:*** ***Always select a heat sink having characteristics that assure T_j will never exceed the maximum junction temperature ($T_{j\,max}$) of the IGBT module(s).***

5.6.3.2 Transient State

Generally, it is sufficient to consider the steady-state junction temperature T_j for radiation design. However, because the power dissipation is actually swinging with pulse state, so that T_j relates to the temperature ripple based on T_c as shown in Figure 38.

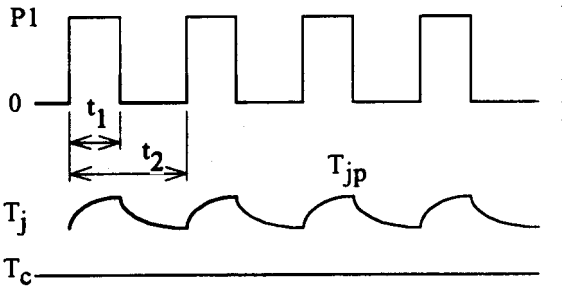


Figure 38. Temperature ripple of T_j

In this case, the ripple peak value of the junction temperature (T_{jp}) can be estimated approximately using Equation 27 and the transient thermal impedance curve of Figure 39.

Equation 27:

$$T_{jp} = P_1 [R_{th}(st) \times (t_1 / t_2) + (1 - t_1/t_2) \times R_{th}(t_1 + t_2) - R_{th}(t_2) + R_{th}(t_1)] + T_c$$

A suitable heat sink should be selected so that T_{jp} will never exceed $T_{j\,max}$.

Figure 39 shows a general representation of transient thermal impedance, and Figure 40 provides an actual example of transient thermal impedance.

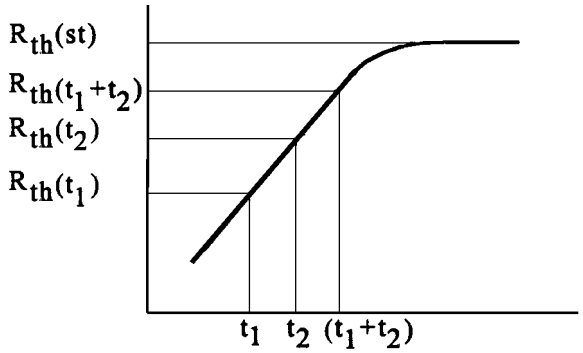


Figure 39. Transient Thermal Impedance

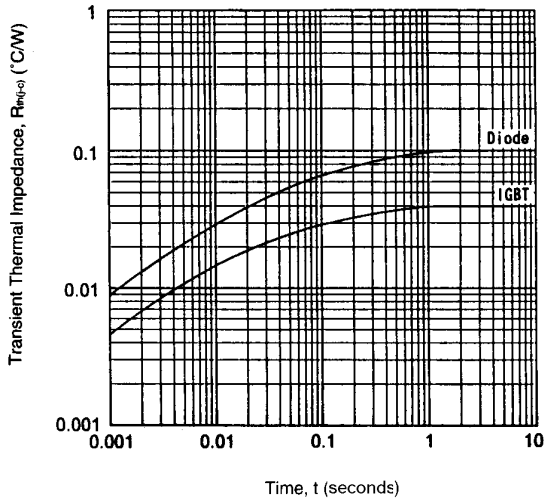


Figure 40. Transient Thermal Impedance Characteristics

5.7 Dead Time

5.7.1 Dead Time Logic in IGBT modules

5.7.1.1 Typical Configuration

Consider an example involving a voltage inverter. Figure 41 shows a single-phase configuration for the top and bottom arms which represents a typical configuration of a major circuit (one phase worth). Top and bottom arms are provided between the P and N of a DC voltage E_o, based on the assumption of a mode where the IGBTs of the top and the bottom arms alternately keep turning ON and OFF. To prevent power supply short-circuiting due to simultaneous ignition (commutation), a top and a bottom IGBT OFF period (dead time) are set using a control signal. This dead time period is also known as the non-lapped period.

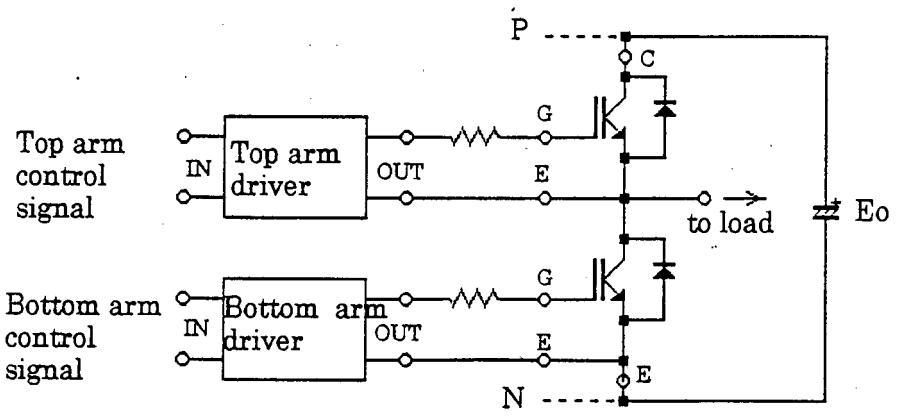


Figure 41. Typical Configuration of a Major Circuit

5.7.1.2 Comparing Dead Time and Real Dead Time

Figure 42 illustrates the various phase relationships among control signal, driver output voltage, and IGBT collector-emitter voltage.

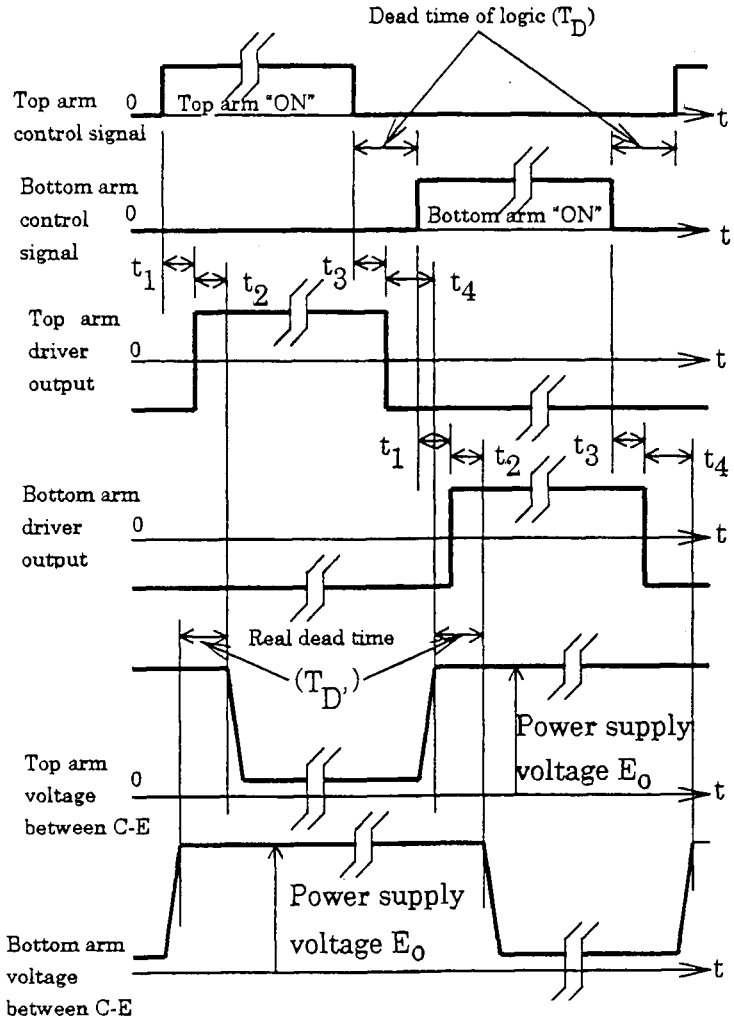


Figure 42. Control Signal, Driver Voltage, and IGBT Collector Voltage Waveforms

Because the dead time (T_D) of the logic circuit deviates due to delays (t_1 and t_3) in Figure 42 in the driver output voltage and switching delays (t_2 and t_4) in the IGBT modules, this situation results in a real dead time referred to as $T_{D'}$ (see below):

Definitions:

- t_1 Output delay time between ON control signal and ON drive voltage
- t_2 Output delay time between ON drive voltage and IGBT turn-ON
- t_3 Output delay time between ON control signal and OFF drive voltage
- t_4 Output delay time and OFF drive voltage and IGBT turn-OFF (provided that, in each of the above cases, there is no difference between the top and bottom arms). The relationship between the dead time (T_D) set on the logic and that of a real dead time ($T_{D'}$) between IGBT and CE are expressed by Equation 28:

Equation 28: $$T_{D'} = T_D - (t_3 + t_4) + (t_1 + t_2)$$

Thus, the dead time (T_D) of the logic circuit changes with the magnitude of the delay times t_1 through t_4 and results in a real dead time ($T_{D'}$).

The next section examines and verifies delays (t_1 and t_3) on the driver line and delays (t_2 and t_4) in the IGBT modules.

5.7.2 Calculating Delay Times of IGBTs

5.7.2.1 Turn-ON and Turn-OFF Switching Waveforms

Figure 43 illustrates the turn-ON and turn-OFF switching waveforms for an inductive load.

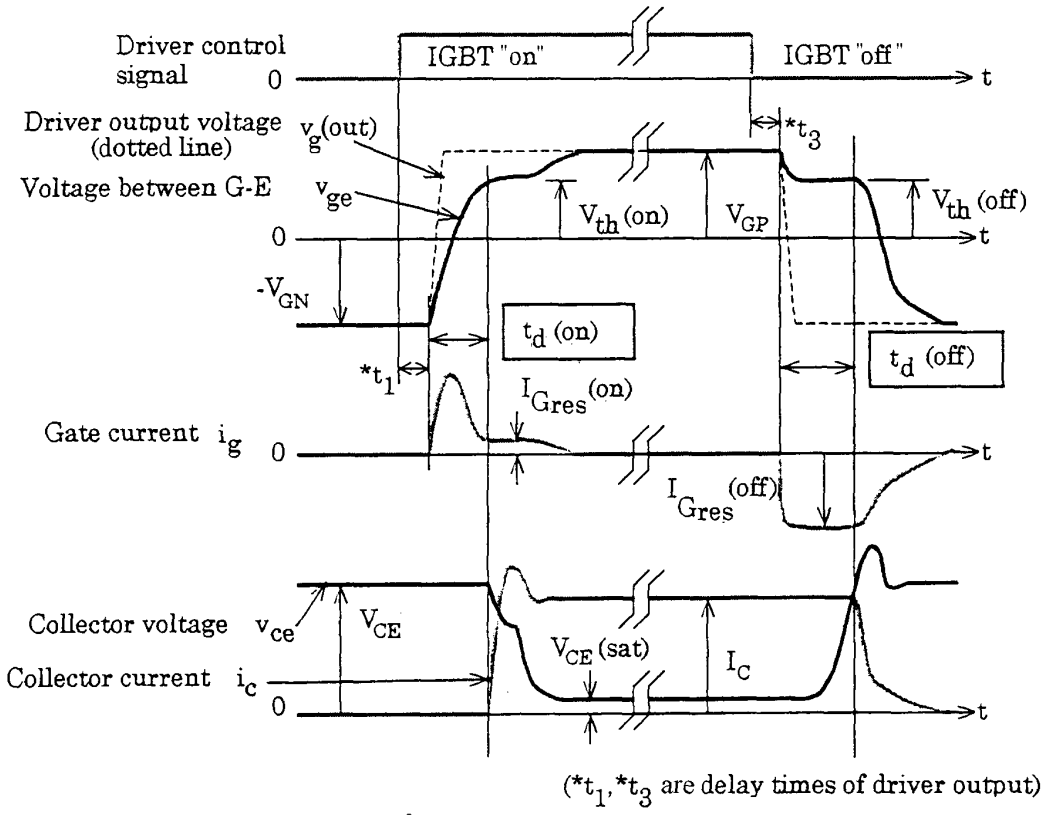


Figure 43. Inductive Load Turn-ON and Turn-OFF Switching Waveforms

5.7.2.2 Calculating Switching Delay Times

Note: ***V_{GP} and V_{GN} in the equations are positive values.***

At turn-ON, driver output voltage v_g (out) changes from $-V_{GN}$ to V_{GP}, the gate input capacitance C_{ies} is charged, the gate voltage (V_{GE}) exceeds the gate threshold voltage (V_{th}), and a collector current (i_c) starts flowing. Immediately after the collector current starts flowing, the gate voltage remains constant at voltage V_{th} (on) determined by collector current I_C for some time (several microseconds) due to effects of reverse transfer capacitance (C_{res}), and discharges return capacitance due to the gate current $I_{G\,res}$ (on) (see Equation 29).

Equation 29: $$I_{G\,res}(on) = (V_{GP} - V_{th}(on))/(R_c + Z_{on})$$

where Z_{on} is the ON-gate voltage output impedance of the driver.

The time until a collector current starts flowing, that is, the turn-ON delay time t_d (on) is given by Equation 30:

Equation 30: $$t_d(on) = -(R_G + Z_{on}) \times C_{ies} [\ln\{(V_{GP} - V_{th}(on))/(V_{GP} + V_{GN})\}]$$

Note: ***Here, t_d (on) is a delay time from the time when the gate voltage is ($-V_{GN}$). If the gate voltage becomes an intermediate voltage due to a narrow control signal input, V_{GN} should be replaced with the intermediate voltage.***

At turn-OFF, it moves to an OFF state due to the discharge of C_{ies}. However, C_{res} is discharged due to the gate current I_{Gres} (off) (see Equation 31) until it becomes constant at the voltage V_{th} (off) where v_{ge} depends only on I_C and the collector voltage v_{ce} becomes source voltage V_{CE}. Collector current I_C declines only when $v_{ce} = V_{CE}$.

Equation 31: $$I_{Gres}(off) = (V_{GP} + V_{th}(off))/(R_G + Z_{off})$$

where Z_{off} is the OFF-gate voltage output impedance of the driver.

The turn-ON delay time is a time t_d (off) until C_{res} is charged to V_{CE} whose value can be determined using Equation 32:

Equation 32:

$$t_d(off) = -(R_G + Z_{off}) \times (C_{ies} + C_{res}(0)) \times \ln\{(V_{GN} + V_{th}(off))/(V_{GP} + V_{GN})\} + Q_{GQ} / I_{Gres}(off)$$

$$= -(R_G + Z_{off})(3 C_{ies}) \times \ln\{(V_{GN} + V_{th}(off))/(V_{GP} + V_{GN})\} + Q_{GQ} / I_{Gres}(off)$$

Definitions:

C_{res} (0)	Reverse transfer capacitance (set equal to 2 C_{ies} here) when V_{CE} is approximately 0V
Q_{GQ}	Total recharging charge (gate charge) of C_{res} (see Figure 44).

Gate charge (parasitic capacitance) of IGBTs

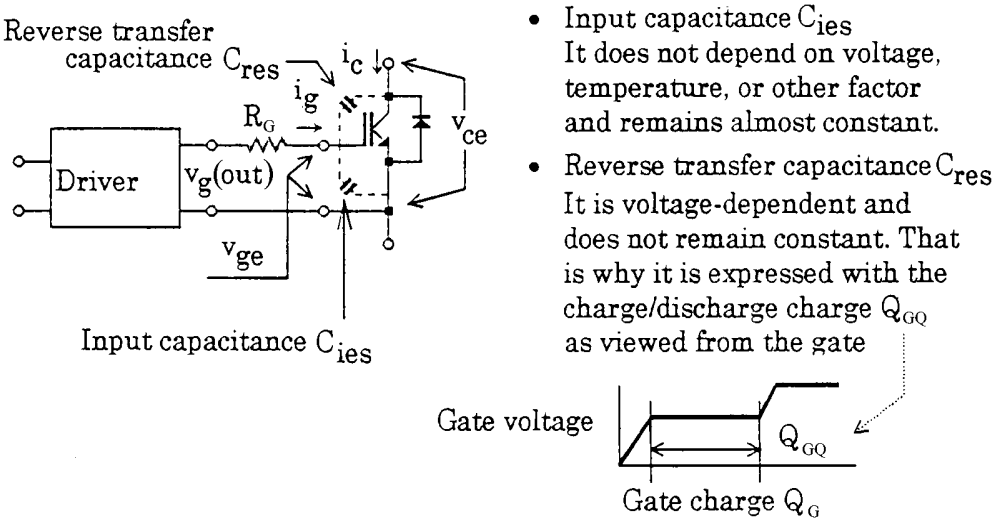


Figure 44. Parasitic Capacitance

5.7.3 Parametric Effects on Switching Delay Time

5.7.3.1 Examining Influential Parameters

Equation 33 allows us to examine the effects of collector current and junction temperature on IGBT module operating conditions:

Equation 33: $$T_{D'} = T_D - (t_3 + t_4) + (t_1 + t_2)$$

Equation 33 provides a means for calculating the real dead time ($T_{D'}$) relative to a dead time (T_D) setting, and this equation allows for finite driver output delays (t_1 and t_3). Often, these particular delay times are judged to be negligible and are set to zero. Realistically, however, all driver delay times must be checked.

The dead times ($T_{D'}$) of IGBT output terminals (C and E) are expressed by Equation 34:

Equation 34: $$T_{D'} = T_D + t_2 - t_4$$

Here, T_D represents a theoretical setting and times t_2 and t_4 are turn-ON and turn-OFF delay times, respectively, which can be determined using Equation 35 and Equation 36.

Equation 35: $$t_d(on) = -(R_G + Z_{on}) \times C_{ies} \times \ln\{(V_{GP} - V_{th}(on))/(V_{GP} + V_{GN})$$

Equation 36: $$t_d(off) = -(R_G + Z_{off}) \times 3C_{ies} \times \ln\{(V_{GN} + V_{th}(on))/(V_{GP} + V_{GN})\} + Q_{GC} / I_{Gres}(off)$$

Substituting these for Equation 34, you will get

Equation 37: $$T_{D'} = T_D [-\{(R_G + Z_{on}) \times C_{ies} \times \ln((V_{GP} - V_{th}(on))/(V_{GP} + V_{GN})\}] -[-\{(R_G + Z_{off}) \times 3C_{ies} \times \ln\{(V_{GN} + V_{th}(off))/(V_{GP} + V_{GN})\}\} + Q_{GC} / (I_{G\,res}(off)]$$

where OFF-gate current $I_{G\,res}$ (off) can be determined with Equation 38:

Equation 38: $$I_{G\,res}(off) = (V_{GP} + V_{th}(off)) / (R_G + Z_{off})$$

Substituting this expression into Equation 37 results in Equation 39:

Equation 39: $$T_{D'} = T_D + [-\{(R_G + Z_{on}) \times C_{ies} \times \ln((V_{GP} - V_{th}(on))/(V_{GP} + V_{GN})\}] -[-\{(R_G + Z_{off}) \times 3C_{ies} \times \ln\{(V_{GN} + V_{th}(off))/(V_{GP} + V_{GN})\}\} + Q_{GC}(R_G + Z_{off}) / (V_{GN} + V_{th}(off)]$$

5.7.3.2 Effect on Gate Voltages

In Equation 39, collector current I_C and junction temperature T_j affect two gate voltages: V_{th} (on) and V_{th} (off) which have a relationship as shown in Figure 45 with collector current.

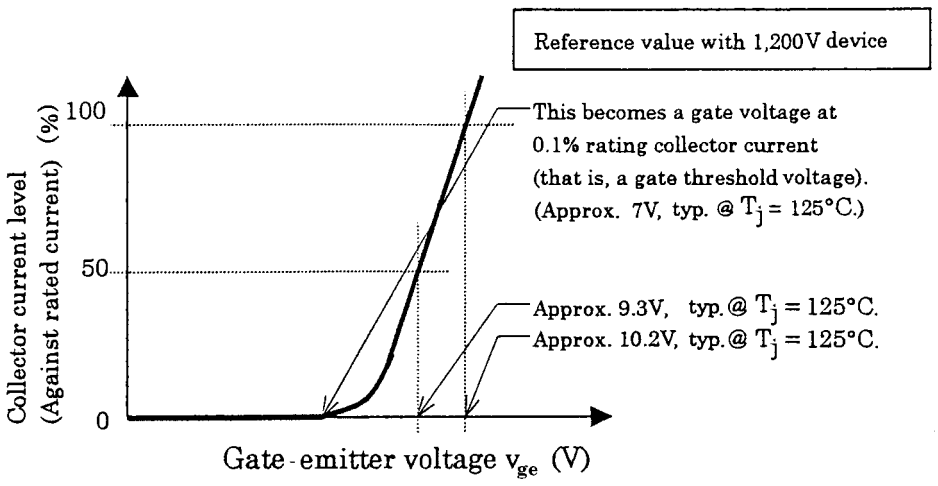


Figure 45. Gate Voltage - Collector Current Characteristics

Figure 45 shows that the gate voltage v_{ge} follows the relationship indicated below (where f_1 and f_2 represent functions):

Equation 40: $v_{ge} \propto f_1(I_C)$

Equation 41: $v_{ge} \propto f_2(1/T_J)$

Here, $T_{D'}$ in Equation 39 is on a downward trend in the case of a low collector current or a high IGBT module junction temperature. In the case of the Hitachi GS Series, it is sufficient to consider (at I_C approximately 0 A and T_j = 125 deg. C.) that V_{th} (on) = 5V and V_{th} (off) = 5V as the bottom limits.

Note: ***1) In a module consisting of IGBT chips in parallel, the gate of each IGBT chip is connected to a resistor chip in series. These resistors are generally composed of semiconductor resistors, so that these temperature factors are rather high: about 1% per degree. If the module has a high temperature, the R_G in Equation 39 becomes equivalently high and the dead time $T_{D'}$ may become short.***

Note: ***2) When extremely narrow control is conducted, and in the case of narrow off control, for example, voltage applied to the gate may not reach the source voltage of the driver, may be applied only at close to 0 Volts, and may be transferred to turn-OFF. Thus, if the gate voltage does not reach the source voltage of the driver, the t_d (on) and t_d (off) can be determined by performing calculations with the V_{GN} and V_{GP} replaced with real values applied to the gate in Equations 35 and 36.***

5.7.3.3 Determinations of Gate Charge Values

The value for Q_{GC} in Equation 39 can be determined for each of the rated collector currents by means of Figure 46.

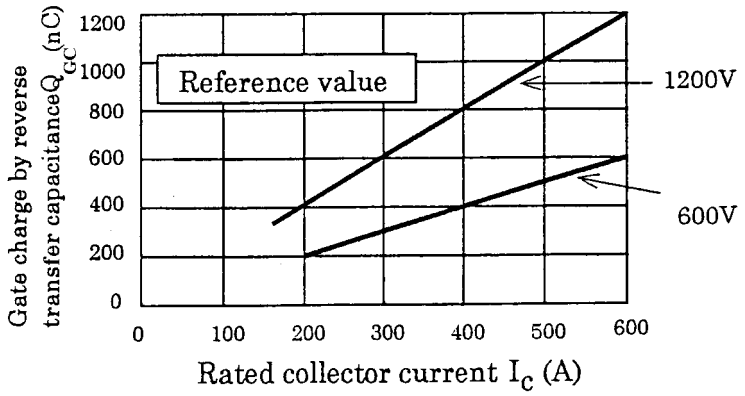


Figure 46. Gate Charge Q_{GC} Values

Because logic dead time varies due to several factors, use dead time values obtained in Equation 39 to establish a setting that assures sufficient leeway.

5.7.3.4 Example of Verification

5.7.3.4.1 Verification Circuit Configuration

Figure 47 shows a half-bridge circuit that will be used to illustrate verification based on an assumption that the top arm turns ON when the collector current of the bottom arm is shut down and a signal is given to the top and the bottom driver circuit.

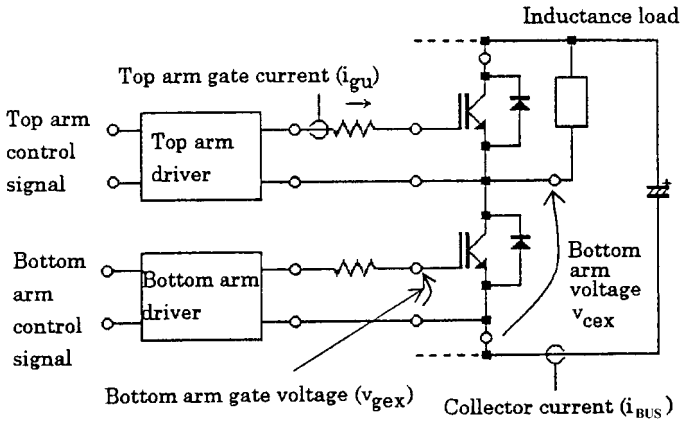


Figure 47. Verification Circuit Configuration

5.7.3.4.2 How to Observe Switching Waveforms

The non-overlap at the top and the bottom arm can be checked in various ways. Special care must be taken when observing voltage waveforms with different potential levels. Any floating-state voltage can be observed with an optical insulation cable or with a differential probe, but these methods require elaborate care concerning delays and other factors. In particular, to observe the gate voltage of the bottom arm with a voltage probe and the gate current of the top arm, a non-contact current transformer (CT) is recommended, such as one manufactured by Pierson (US).

5.7.3.4.3 How to Check Vertical Motion

Figure 48 represents waveforms observed at the time of the verification. The turn-OFF of the bottom arm is regarded as the point (Point B) where the gate voltage starts shifting to a reverse bias, and the phase relationship between it and the peak point (Point A) of the gate current of the top arm is used to determine whether overlap or non-overlap is present.

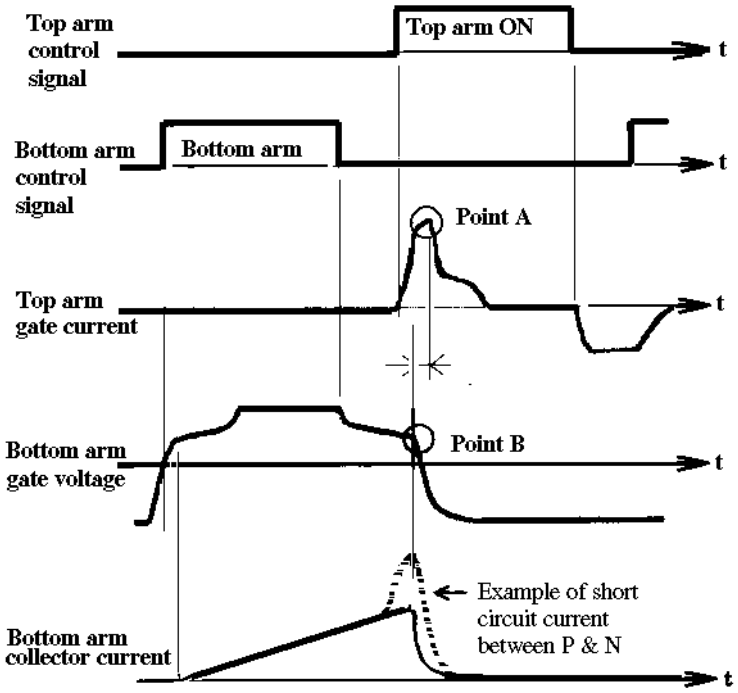
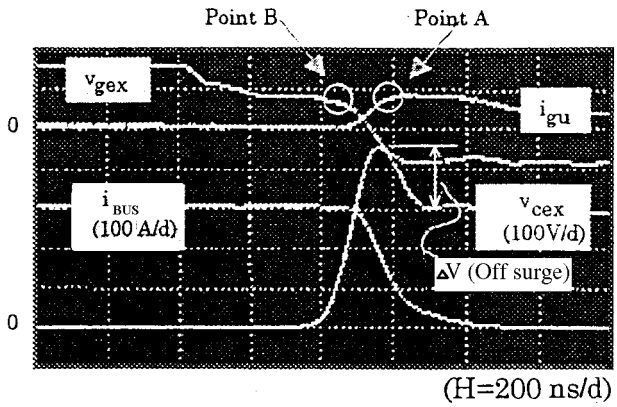
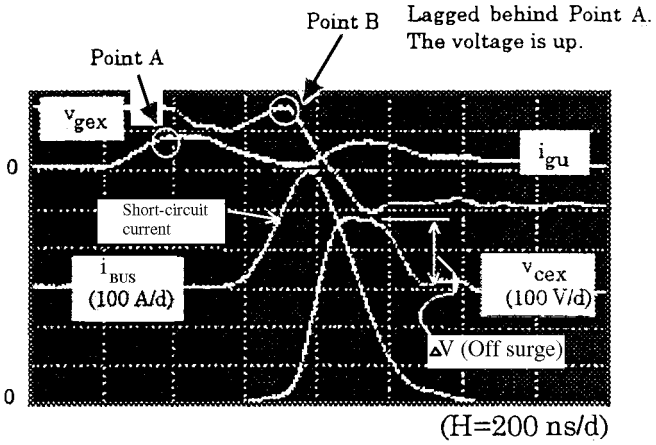


Figure 48. Control Signal and Gate Waveforms

If Point A occurs earlier than does Point B, the top and bottom arms can be considered to be short-circuited. (See Figure 48.) When the top and bottom arms are short-circuited, collector current becomes something like what is indicated by broken lines in Figure 48, with a rise in switching loss. In the gate voltage waveform at this time, a rise in Point B voltage is observed. (If significant short-circuiting arises, the system shifts from gate source voltage to reverse bias voltage.)



(1) Top and bottom not short-circuited



(2) Top and bottom short-circuited

Figure 49. Top and Bottom Arm Waveforms

5.7.3.4.4 Typical Verification

Figure 49 represents how a typical verification can be conducted in a circuit configuration as shown in Figure 47 and in waveform observations in Figure 48. This example is based on a 600 V, 300 A IGBT module and has been observed with the control signal phase of the top arm changed. Figure 49 (1) shows the no short-circuiting situation, while Figure 49 (2) reflects the short-circuited top and bottom arms condition.

5.8 Short Circuit Protection

5.8.1 Short Circuit Pattern

The short circuit pattern in the inverter can occur in two ways:

(1) In the inverter side (due to IGBT module destruction, control circuit trouble, equipment ground fault, etc.)

(2) In the load side (due to connection error, load trouble, ground fault, etc.)

5.8.2 IGBT Operation during Short Circuit

When the short circuit occurred, in the case where an IGBT is maintained in either the ON steady state or turn-ON state, the short-circuit current increases up to the IGBT's saturation current. (This current increases up to approximately six (6) times the rated current.) Also, almost the entire circuit voltage is applied to the IGBT. If such a status occurs continuously, the IGBT will be destroyed. To prevent this phenomenon, the short-circuit current must be cut off before the onset of IGBT destruction is approached.

5.8.3 Short-circuit Current Cut-off

To prevent IGBT destruction, whatever protection method is chosen must cut off the current within 10 microseconds after short-circuit current has begun to flow. See Figure 50. Two cut-off protection methods and their respective features are described below.

5.8.3.1 Hard Cut-off

Method: IGBT normally turns OFF after detecting an over-current. Such monitoring of over-current would be performed using a Current Transformer (CT), etc.

Feature: Only current detecting. Large turn-OFF overshoot voltage.

Note: The circuitry needs to control overshoot voltage. In cases where the line impedance is large, precautions should be taken to prevent the snubber circuit voltage from increasing.

5.8.3.2 Soft Cut-off

Method: The gate voltage is controlled after detecting the overcurrent. The driver circuit monitors V_{CE} (sat) increasing and controls gate voltage.

Feature: Small overshoot voltage. Driver needs the monitoring function of V_{CE} of one arm in order to be able to see the troubled arm.

Note: It is necessary to properly set up detection delay in order to be able to observe this behavior during a normal IGBT turn ON operation.

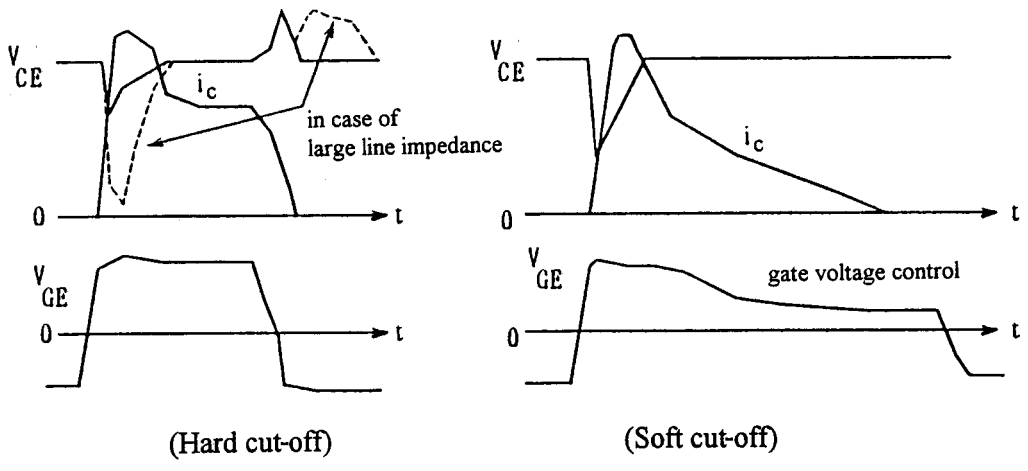


Figure 50. Short-circuit Protection Waveforms

5.8.4 Short-circuit Current and Gate Voltage Increase

Collector voltage increases with short-circuit current, at the same time gate voltage increase due to dv/dt current flows to gate through reverse transfer capacitance (C_{res}). The increase in gate voltage can be estimated by examination of the Q_{res} electric charge characteristics. (Refer to Figure 51.)

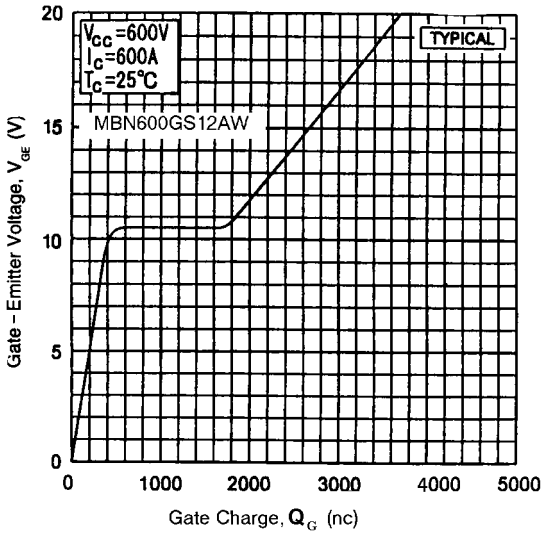


Figure 51. Example of Gate Charge Characteristics

Figure 52 represents a standard drive circuit for an IGBT and its connection. When the IGBT's collector voltage increases due to short circuit current, Q_{res} conducts to the gate through C_{res}.

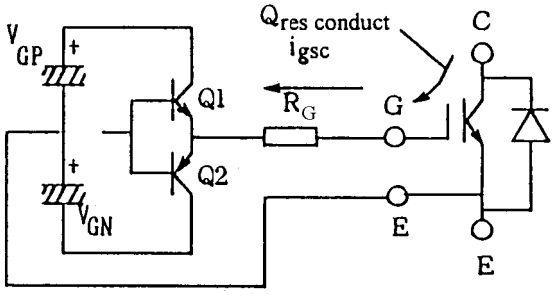


Figure 52. Dependency of Gate Voltage upon C_{res}

In this case, gate current (i_{gsc}) can be calculated as shown in Equation 42.

Equation 42: $$i_{gsc} = (v_{ge}(i) - V_{GP}')/R_G$$

and Q_{res} can be calculated using Equation 43:

Equation 43: $Q_{res} = i_{gsc} \times t_{scv}$

Definitions:

$v_{ge}(i)$	Gate voltage of IGBT
V_{GP}	Terminal voltage of driver output (approx. 16V)
i_{gsc}	Gate current from gate to driver
t_{scv}	Collector voltage increase term (approximately 3 to 5 μs).

The IGBT gate voltage ($v_{ge}(i)$) can be calculated using Equation 44.

Equation 44: $v_{ge}(i) = Q_{res} \times R_G / t_{scv} + V_{GP'}$

For example,

$V_{GP'}$	= 16 V
Q_{res}	= 700 nC (for an MBM300GS12A device)
R_G	= 4.3 ohms
t_{scv}	= 3 μs
$v_{ge}(i)$	= 17 V (approx.)

5.8.5 Prevention of Gate Voltage Increase

Saturation value of short circuit current increases with gate voltage increase, especially in the hard cut-off method for short-circuit protection. Also, overshoot voltage increases with cut-off current increase.

To prevent gate voltage increase, use the following approach.

(1) Connect a diode from emitter toward the collector of transistor (Q1) to bypass the current. Especially for the case involving the hard cut-off method, the emitter follower output circuit is not necessary, as the CMOS output circuit is already an effective means. (Note that there is an inner diode in the MOSFET.)

(2) Connect in series the zener diode and diode between gate (G) and emitter (E) terminals.

6 Handling

6.1 Mounting IGBT modules to Heat Sinks

6.1.1 Clamping Torque

Table 6 lists recommended clamping torque values.

Table 6. Clamping Torque

No	Screw	Rated Torque (N-m)	Recommended Torque (N-m)	Pre-clamping Torque (N-m)	Final clamping Torque (N-m)
1	M5	1.96	1.67	0.33 to 0.55	1.67
2	M6	2.94	2.45	0.49 to 0.8	2.45

6.1.2 Thermal Compound Grease

Apply thermal compound grease between the IGBT module and heat sink as explained below.

(1) First apply grease on the base side of module. Do this by roller/ brush or placing of grease of uniform quantity at several points (see Figure 53). Table 7 shows the recommended grease and its specific gravity. The recommended thickness of grease should be in the range of 100 μm to 150 μm. For example, the quantity of grease required (q) can be estimated using Equation 45.

Equation 45: $q = s \times t \times k$

Definitions:

S (cm^2)	Base area of module
t (cm)	Thickness of grease
k (kg/cm^3)	Specific gravity of grease

For the case of three (3) points applying method, each point quantity should be 1/3 of the total quantity of grease required. For the case of five (5) points, should be 1/5 of the total quantity of grease required.

(2) Next, push the base side of the IGBT module against the heat sink, particularly since such grease has a tendency to spread to all surfaces.

(3) Mount the IGBT module according to the clamping order of screw shown in Figure 54 or Figure 55 accordingly. Take note of the stated clamping torque as given in Table 9. In particular for the case where an electromotive driver is used, take care to preclude clamping beyond the maximum specified torque.

Note: ***It is not necessary to allow for any rest time between pre-clamping and final clamping activities.***

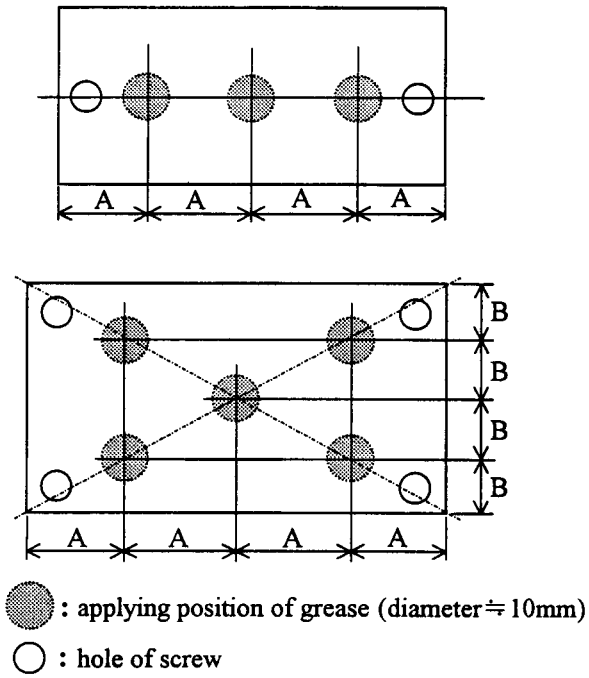


Figure 53. Grease Positions

Table 7. Recommended Grease and Specific Gravity

No.	Manufacturer	Type	Specific Gravity
1	Shinetsu Kagaku Co.	G746	2.66 g / cm^3
2	Toshiba Silicone Co.	YG6260	2.5 g / cm^3

6.1.3 Clamping Order of Screws

Figures 54 and 55 illustrate the recommended order for clamping of mounting screws.

Note: The recommended starting point is not indicated on IGBT modules.

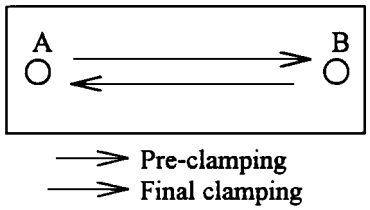


Figure 54. Clamping Order for Two-point Clamping Module

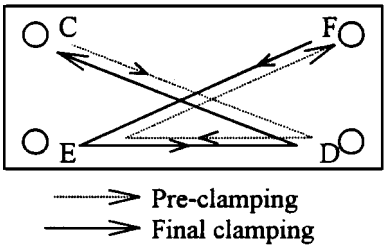


Figure 55. Clamping Order for Four-point Clamping Module

6.1.4 Surface Roughness and Warp of Heat Sink

(1) The surface roughness of the heat sink should not be less than ∇∇ (25S).
(2) The convex or concave warp of heat sink should not be more than 100 μm (between the mounting screw holes).
(3) Confirm that the surface of the heat sink is free of burrs. Be sure to chamfer the screw holes.
(4) Always be certain to look for and remove all foreign substances, such as cut chips, which may get caught between the IGBT module and heat sink.

6.1.5 Heat Sink Mounting Hole Diameter

Select the mounting hole diameter suited to the screw to be used.

Note: ***If the heat sink mounting hole diameter is too large, the module's base may be deformed and the dice in the module damaged as shown in Figure 56.***

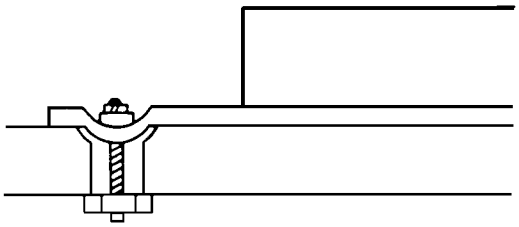


Figure 56. Example of Improper Heat Sink Mounting

Table 8 shows the mounting hole diameter for the screw size to be used and the recommended chamfering value.

Table 8. Recommended Mounting Hole Diameter and Chamfering Value

No.	Screw	Mounting Hole Diameter (in mm.)	Recommended Chamfering Value (in mm.)
1	M4	φ5	C 0.5
2	M5	φ6	C 0.5
3	M6	φ7.5	C 0.5
4	M8	φ9.5	C 0.5

6.2 Main Terminal

6.2.1 Pre-clamping and Final Clamping of Main Terminal

Pre-clamping for connecting of main terminal and main circuit line is not necessary.

6.2.2 Recommended Clamping Order of Mounting Screws

The clamping order of mounting screws for the IGBT's main terminal is not critical.

6.2.3 Clamping Method for Mounting Screws

Table 9 lists values for the mounting screw clamping torque. Use of either a hand- or electromotive-driver tool is recommended for such operations.

Table 9. Recommended Clamping Torque for Terminals

No.	Screw	Rated Torque (N-m)	Recom-mended Torque (N-m)	Minimum Torque (N-m)	Remarks
1	M4	1.37	1.18	0.98	for auxiliary terminal
2	M5	1.96	1.67	1.47	
3	M6	2.94	2.45	1.96	
4	M8	7.84	7.35	5.20	

6.2.4 Recommended Screw Length

Figure 57 shows cross sectional view of the screw hole in the module side. The recommended screw length is such that "d" dimension extends one to two millimeters below the nut.

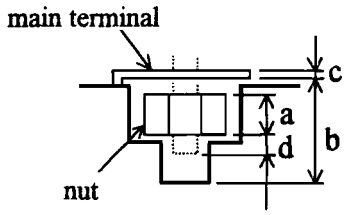


Figure 57. Cross-sectional View of Screw Hole

Table 10 shows the hole size for each screw, but these dimensions do not include the thickness of bus-bar and other items.

Table 10. Size for Screw Hole

Screw	a (in mm.)	b (in mm.)	c (in mm.)	Remarks
M4	3.2	7.0	0.8	for auxiliary terminal
M5	4.0	8.5	1.2	
M6	5.0	10.0	1.2	
M8	6.0	10.0	1.2	

6.3 Mounting Precautions

6.3.1 Fast-On Terminal

The signal terminal (gate-to-emitter terminal) of the IGBT module has a fast-on terminal structure. This terminal should not experience a tension exceeding 0.46 N (4.5 kg - f) and should never be bent in a crosswise direction.

Take the following precautions when soldering the terminals.

(1) 60-watt soldering iron and soldering contact time of less than 5 seconds.
(2) Pb:Sn (40:60) eutectic solder (melting point of 180 degrees Celsius)
(3) rosin flux

6.3.2 Environmental

6.3.2.1 Harmful Substances

When an IGBT module is exposed to corrosive gases, such as sulfur dioxide or chlorine gas, conductivity or heat radiation may decrease because of terminal or base corrosion and parts may discolor. Make sure to always keep IGBT modules away from such substances.

6.3.2.2 Exposure to Elements

Protect the IGBT module from both rain and water.

6.4 Storage and Shipping Considerations

6.4.1 Recommended Storage Conditions

IGBT modules should always be stored under the following conditions.

(1) Temperature: 40 degrees Celsius, maximum.
(2) Humidity: 60% Relative Humidity, maximum.
(3) Dust: Avoid storing the module in locations subject to dust.
(4) Harmful substances: The installation location should be free of corrosive gases such as sulfur dioxide and chlorine gas.
(5) Stacking: Avoid overstacking, as the signal gate and emitter terminal may be crushed.
(6) Other: Do not remove the conductive sponges or tapes attached to the signal gate and emitter terminal.

6.4.2 Shipping Method

(1) To prevent the case cracking and/or the electrode bending, appropriate consideration should be given to properly insulate the shipping container from mechanical shock or severe vibration situations.

(2) Appropriate labeling on the outside of the shipping container should always be present.

(3) The shipping container itself should always be properly protected from both rain and water.

6.5 Precautions against electrostatic failure

Because the IGBT has a MOS gate structure, you should always take the following precautions as measures to avoid generating static electricity.

a) Before starting operation, do not remove the conductive sponge or tape mounted between gate and emitter.

b) When handling the IGBT module, ground your body via a high-value resistor (between 100 Kilohm and 1 Megohm), hold the package body, and do not touch the gate terminal.

c) Be sure to ground any parts which the IGBT module may touch, such as the work table or soldering iron.

d) Before testing or inspection, be sure to check that any residual electric charge in the measuring instruments has been removed. Apply voltage to each terminal starting at 0V and return voltage to 0V when finishing.

6.6 IGBT Module Circuit Arrangement and Wiring Method

Arrange the IGBT module as close to the power source as possible. Because excessive voltage applied to the IGBT module will result in device breakdown, remember to keep the cable between the gate circuit and IGBT module as short as possible. If this is not done, gate voltage will rise or fall more slowly and the switching time will become longer.

If the cable between the power source and the IGBT module becomes too long, cable inductance will generate an overshoot voltage, especially when the module is turned OFF. In addition, the likelihood of noise generation will be increased. Alternatively, to prevent a long gate cable from experiencing noise easily, either two-wire stranded cable or shielded cable should be used.

6.7 Measurement Precautions

a) Before beginning V_{CES} measurements, be sure to short-circuit the signal gate and emitter terminals.

Note: ***If the signal gate and emitter terminals are kept open or their contact is defective during measurement, the IGBT module may be damaged.***

b) Within the IGBT module, a cable is laid between the chip in the module and the external connection terminal. The voltage applied to the chip and the voltage of the external terminal are not identical, especially during switching.

For expressing the time rate of change in current as di/dt and the cable inductance as L, an inductive voltage equal to L di/dt will be generated within the cable. Typically, cable inductance L is about 20 to 40 nH. so when the IGBT module is turned ON, the external terminal voltage observed is higher than the voltage applied to chip.

Conversely, when the IGBT module is turned OFF, the observed external terminal voltage is lower than the voltage applied to the chip.

c) The voltage applied to the chip should not be permitted to exceed the rated voltage of the device.

7 Reliability

7.1 Module Failure Regions

Figure 58 shows the generalized failure rate behavior of Hitachi IGBT modules. Historically, such a "bathtub-shaped" curve is sectioned into three regions, namely:

A: Infant mortality

B: Premature failure

C: End-of-life failure

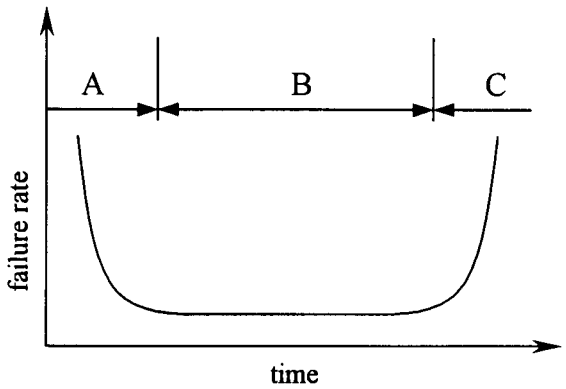


Figure 58. Module Failure Regions

7.2 Failure Factors

Table 11 categorizes IGBT module failure factors and includes examples for each failure category.

Table 11. Failure Mechanisms

Failure Factor	Examples
Materials and structures of parts	1) Chemical interactions among metals or with die 2) Mismatching of thermal expansion rate
Deviation in Product Process	1) Failure of Al wire bonding 2) Scar of die surface pattern 3) Failure of air-tight packaging 4) Failure of solder
Thermal Stress	1) Destruction due to thermal expansion 2) Die destruction due to exceeding isolation voltage
Electrical stress	1) Package destruction due to exceeding isolation voltage 2) Die destruction due to exceeding isolation voltage
Mechanical Stress	1) Connection bending 2) Package cracking
Chemical Stress	Corrosion of outer electrode Rusting of terminals
Radiation	Change in device electrical characteristics due to accumulation of surface electric charge

7.3 Quality Tests

Table 12. Tests and Methods

Test #	Type of Test	Test Methods and Descriptions
1	Temperature cycling	Through all rating storage temperature range: 50 cycles
2	Thermal shock	Prepare two liquid baths: one @ minimum storage temperature; another @ maximum storage temperature. Quickly put samples into each bath temperature. Holding time: 5 minutes each temperature. No. of cycles: 5 cycles in Fluorinert liquid.
3	Mechanical Shock	Acceleration: 500 G (where G equals the force of gravity). Time: 1 millisecond. Direction: X, Y, and Z (for 3 times).
4	Mechanical Vibration	Acceleration: 10 G (where G equals the force of gravity). Frequency: 100 Hz through 2 kHz. Sweep time: 20 minutes per cycle. Direction: X, Y, and Z Time: 6 hours.
5	Screw torque	Torque: Twice the rated torque. Storage: 336 hours.
6	Fast-on strength	Tensile strength: 44.1 Newtons (for MBM300GS6A) Storage time: 30 seconds
7	Intermittent operating life	Place on heat sink and apply power to the samples. Current waveform: 60 Hertz half sine wave. Peak Current (I_p): Rated I_C of module. Temperature swing: ΔT_C = 70 degrees Celsius. Duration: 5,000 cycles.
8	Applied DC voltage	Voltage: 0.8 times rated V_{ce} . Time: 1,000 hours Temperature: 125 degrees Celsius.
9	Applied AC voltage	Peak voltage: 0.8 times rated V_{ce} . Time: 1,000 hours. Test temperature: 125 degrees Celsius.
10	High-temperature storage	Temperature: Maximum storage temperature. Storage time: 1,000 hours.
11	Low-temperature storage	Temperature: Minimum storage temperature Storage time: 1,000 hours.
12	High humidity	Humidity: 90% Relative Humidity (RH). Temperature: 60 degrees Celsius. Time: 1,000 hours.

7.3.1 Examples of Possible Failure Mechanisms

Figure 59 shows a graphical representation for possible failure mechanisms within an IGBT module.

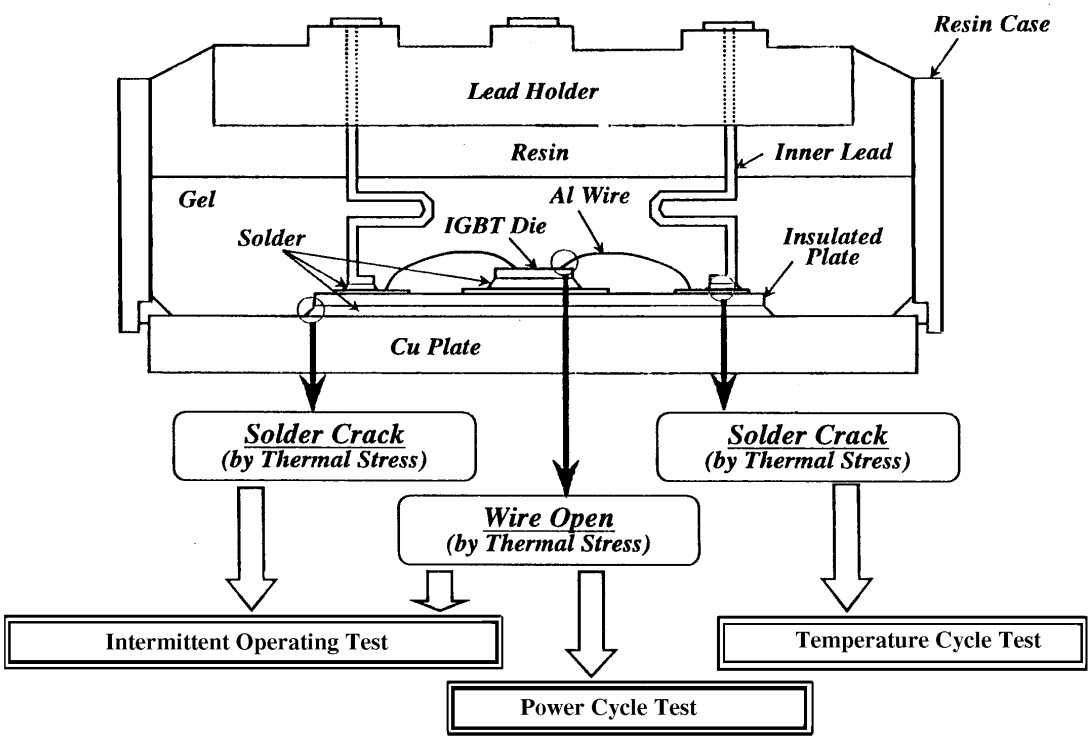


Figure 59. Possible Failure Mechanisms for an IGBT Module

7.3.2 Acceptable Characteristics Limits after Quality Testing

(1) I_{ces} , I_{ges} < 2.0 times rated value.
(2) V_{ce} (sat), V_f < 1.2 times rated value.
(3) R_{th} (j - c) < 1.5 times rated value.

7.3.3 Sample Testing Criteria

(1) Number of Samples --- 6 pieces for each test
(2) Number of Rejects --- 0 Rejects allowed

7.3.4 Frequency of Sample Testing

(1) Initial development stage for final design (Type test)
(2) Once per final design module, substitute similar design modules data for module testing result.

7.3.5 Test results

Table 13 shows a representative example for a specific IGBT module (Type No.: MBM300GS6A with ratings: 600 V / 300 A, T_j = - 40 to 125 deg C.)

Note: Acceptable limits after testing depend on section 7.3.2.

Table 13. Representative Example of Test Results

No.	Type of Test	Test Conditions	Sample Size	No. of Failures	Judgment
1	Temperature cycling	Temperature Range: -40 to 25 to 125 deg C Holding time: 30 minutes each temperature No. of cycles: 50 cycles	6	0	pass
2	Thermal shock	Temperature Range: -40 to 125 deg C Holding time: 5 minutes each temperature. No. of cycles: 5 cycles in Fluorinert liquid	6	0	pass
3	Mechanical Shock	Acceleration: 500 G (where G equals the force of gravity). Time: 1 millisecond. Direction: X, Y, Z --- 3 times each.	6	0	pass
4	Mechanical Vibration	Acceleration: 10 G. Frequency: 100 Hz through 2 kHz. Sweep time: 20 minutes per cycle. Direction: X, Y, Z --- 6 hours each.	6	0	pass
5	Screw torque	Torque: 3.92 N-m Storage: 336 hours	6	0	pass
6	Fast-on strength	Tensile Strength: 44.1 N Storage: 30 seconds.	6	0	pass
7	Intermittent operating life	Current: 60 Hz half sine-wave. I_{peak} = rated I_C of module. Temperature swing: ΔT_C = 70 degrees Celsius. No. of cycles: 5,000	6	0	pass
8	Applied DC voltage	Applying voltage: 0.8 x rated V_{CE} . Time: 1,000 hours. Temperature: 125 degrees Celsius.	6	0	pass
9	Applied AC voltage	Applying peak voltage: +/- rated V_{GE} . Time: 1,000 hours. Temperature: 125 degrees Celsius.	6	0	pass
10	High-temperature storage	Temperature: 125 degrees Celsius. Time: 1,000 hours.	6	0	pass
11	Low-temperature storage	Temperature: - 40 deg C. Time: 1,000 hours.	6	0	pass
12	High humidity	Humidity: 90% Relative Humidity (RH). Temperature: 60 degrees Celsius. Storage: 1,000 hours.	6	0	pass

8 Troubleshooting

8.1 Electrical Failure Analysis

The electrical failure analysis diagram for analyzing breakdown of an IGBT module is illustrated on the next two facing pages (refer to Figure 60).

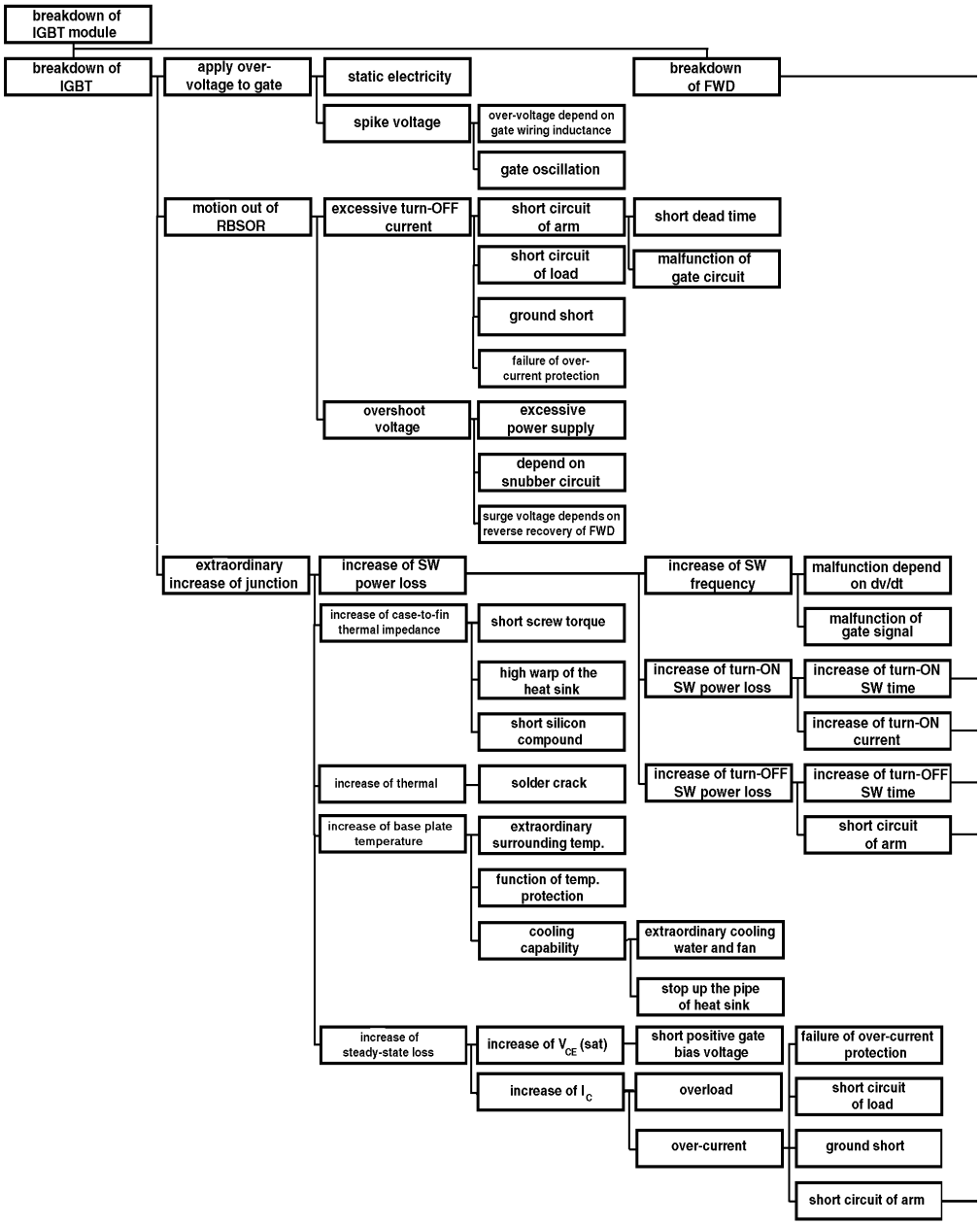
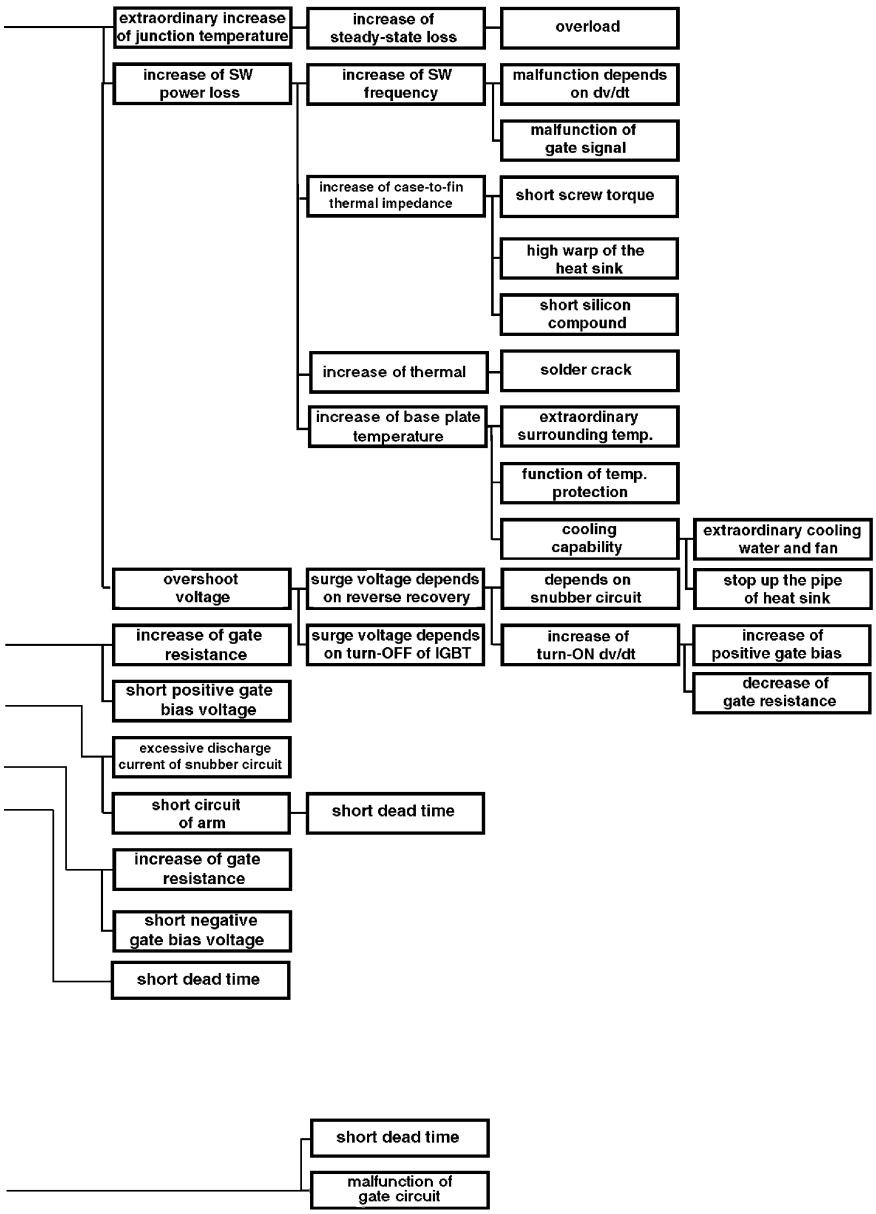


Figure 60. Electrical Failure Analysis


extraordinary increase of junction temperature
increase of steady-state loss
overload
increase of SW power loss
increase of SW frequency
malfunction depends on dv/dt
malfunction of gate signal
increase of case-to-fin thermal impedance
short screw torque
high warp of the heat sink
short silicon compound
increase of thermal
solder crack
increase of base plate temperature
extraordinary surrounding temp.
function of temp. protection
cooling capability
extraordinary cooling water and fan
stop up the pipe of heat sink
overshoot voltage
surge voltage depends on reverse recovery
depends on snubber circuit
surge voltage depends on turn-OFF of IGBT
increase of turn-ON dv/dt
increase of positive gate bias
decrease of gate resistance
increase of gate resistance
short positive gate bias voltage
excessive discharge current of snubber circuit
short circuit of arm
short dead time
increase of gate resistance
short negative gate bias voltage
short dead time
short dead time
malfunction of gate circuit

8.2 Device Check Method

To check IGBT electrical characteristics, a "Curve Tracer" is generally used to measure voltage and current. Figure 61 shows both good and bad sample examples for checking IGBT module characteristics.

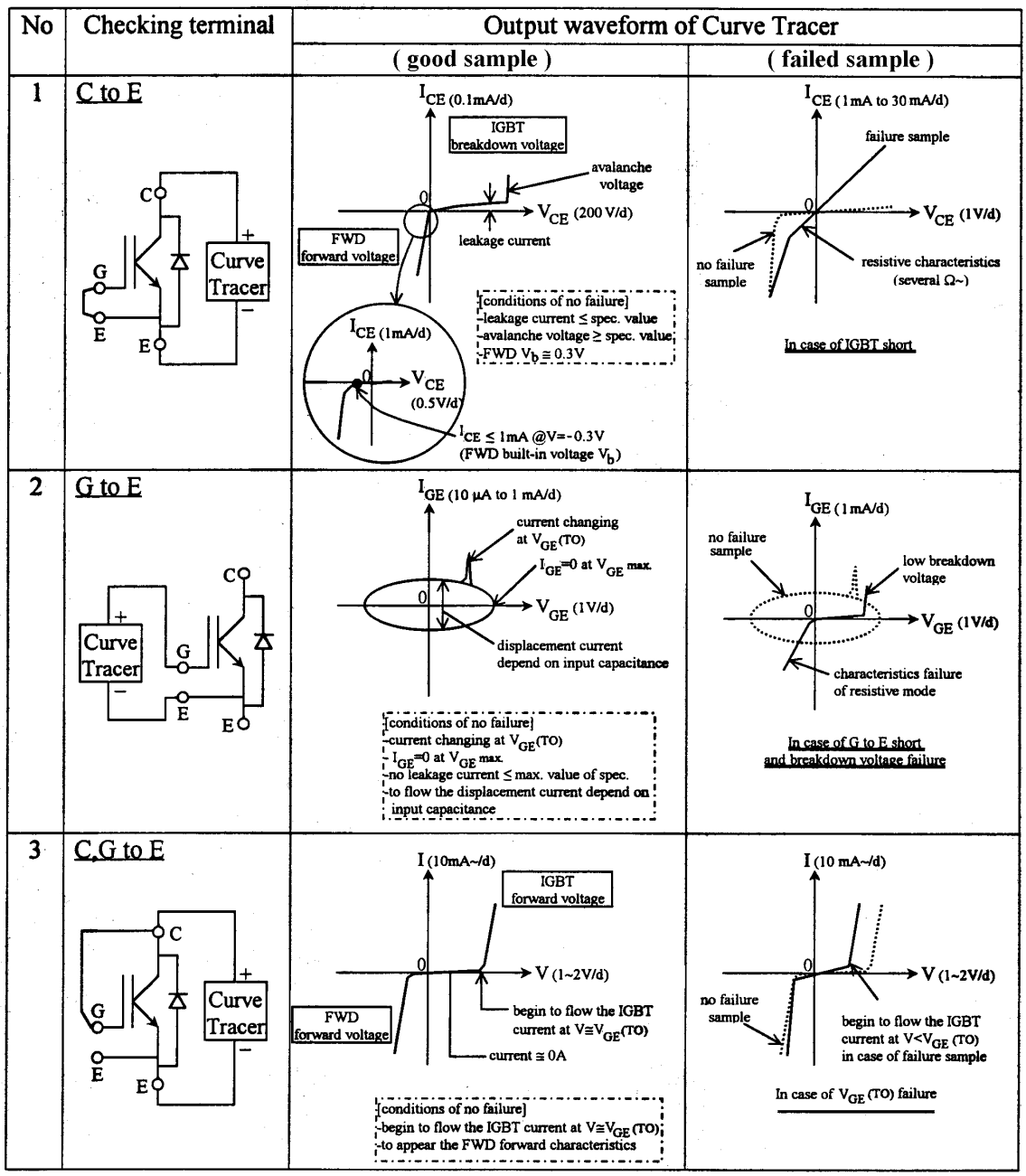


Figure 61. Curve Tracer-based IGBT module Checking

Note: ***In the above Figure, an AC measurement mode of Curve Tracer is used. You may wish to use DC mode to make it easier to observe leakage failure due to the low displacement current.***

9 Failure Precautions

WARNING

When either a load- or arm- short circuit occurs in an IGBT module, it must be turned OFF immediately. Otherwise, the module case may burst because energy at the time of short circuit accumulates in the module and will be released instantaneously.

Always be certain that you take the following precautions:

1) Keep the IGBT module in a closed case to prevent operator harm should it ever burst.
2) Never open the IGBT module's closed case while an electric current is being supplied to the module.

CAUTION

To avoid emission of smoke or a fire to be initiated, recognize that a short-circuit current must never be allowed to flow for any extended period of time after the IGBT module fails.

Note: Although IGBT modules use fire-retardant material, such as UL94VO, you should always make use of fuse-based circuitry to protect the module.